

8

7

6

5

4

3

2

1

1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.

2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.

3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

SCHEM, MLB, M1

Post Ramp Revision07/14/2006

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REV

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ECN

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TPM

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Revision History

N/A

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(MASTER)

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ANGLED CAPS FOR C4 NOISE

N/A

051-7181

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SCHEM, MLB-RP, M1

SCH

CRITICAL

820-1881

1

PCBF, MLB, M1

PCB

CRITICAL

SCHEM, MLB, M1

07/14/2006

051-7181

B

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OF

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DIMENSIONS ARE IN MILLIMETERS

XX ±

X.XX ±

X.XXX ±

ANGLES ±

DO NOT SCALE DRAWING

THIRD ANGLE PROJECTION

METRIC

DRAFTER

ENG APPD

QA APPD

RELEASE

MATERIAL/FINISH NOTED AS APPLICABLE

DESIGN CK

MFG APPD

DESIGNER

SCALE

SIZE

NONE

D

Apple Computer Inc.

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SCHEM, MLB, M1

DRAWING NUMBER

051-7181

REV.

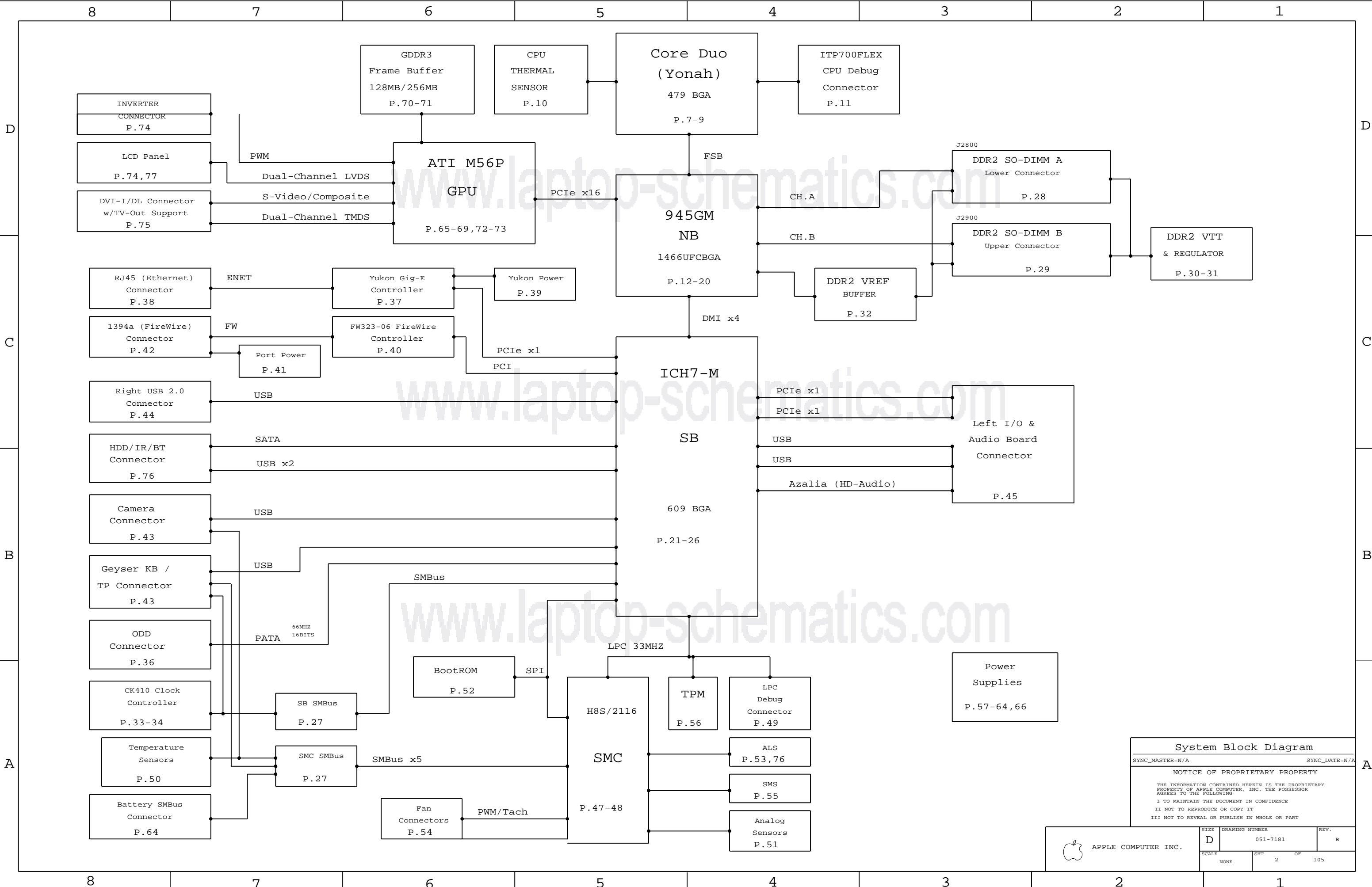
B

SHT

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**System Block Diagram**

SYNC\_MASTER=N/A SYNC\_DATE=N/A

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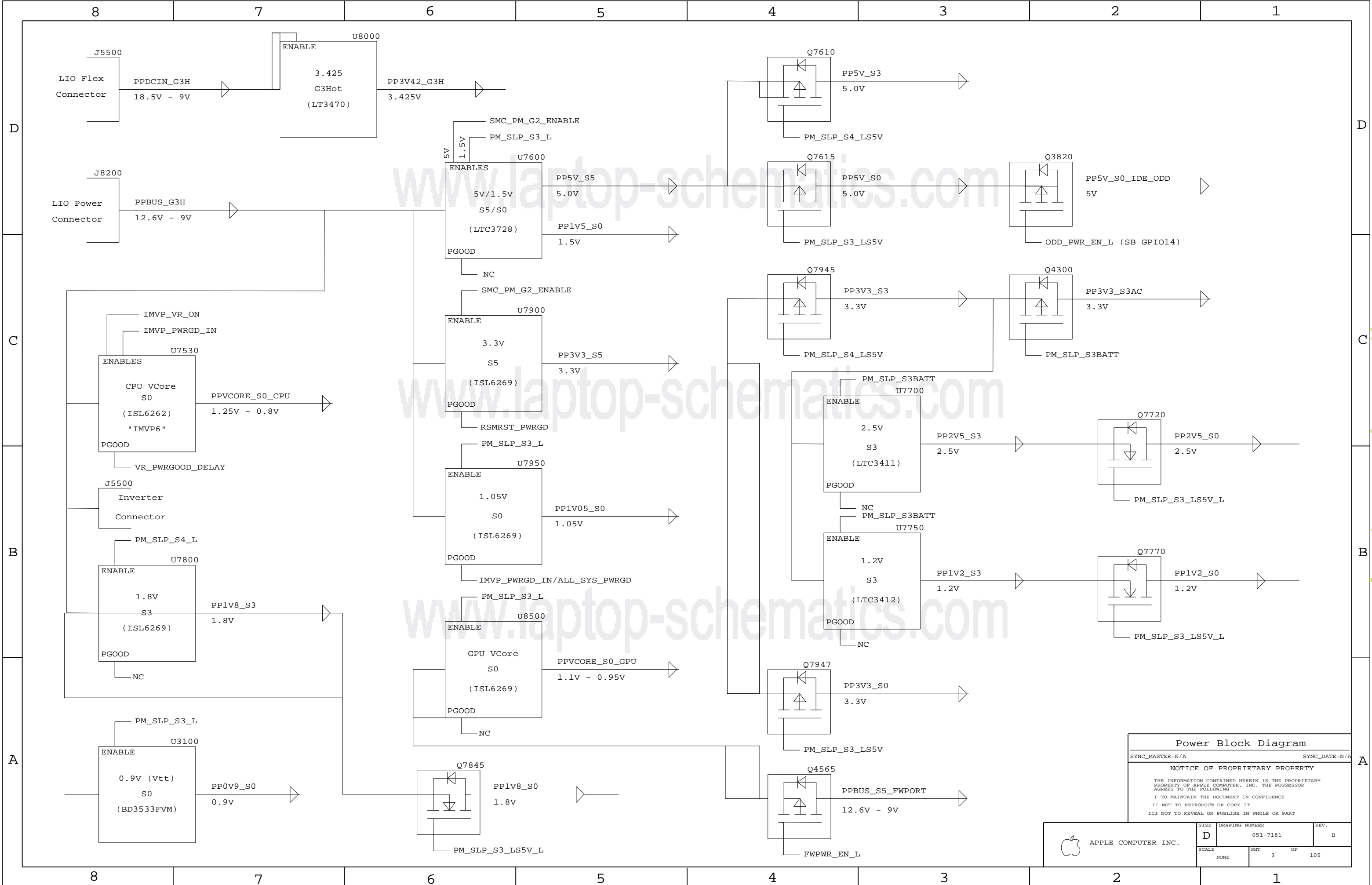
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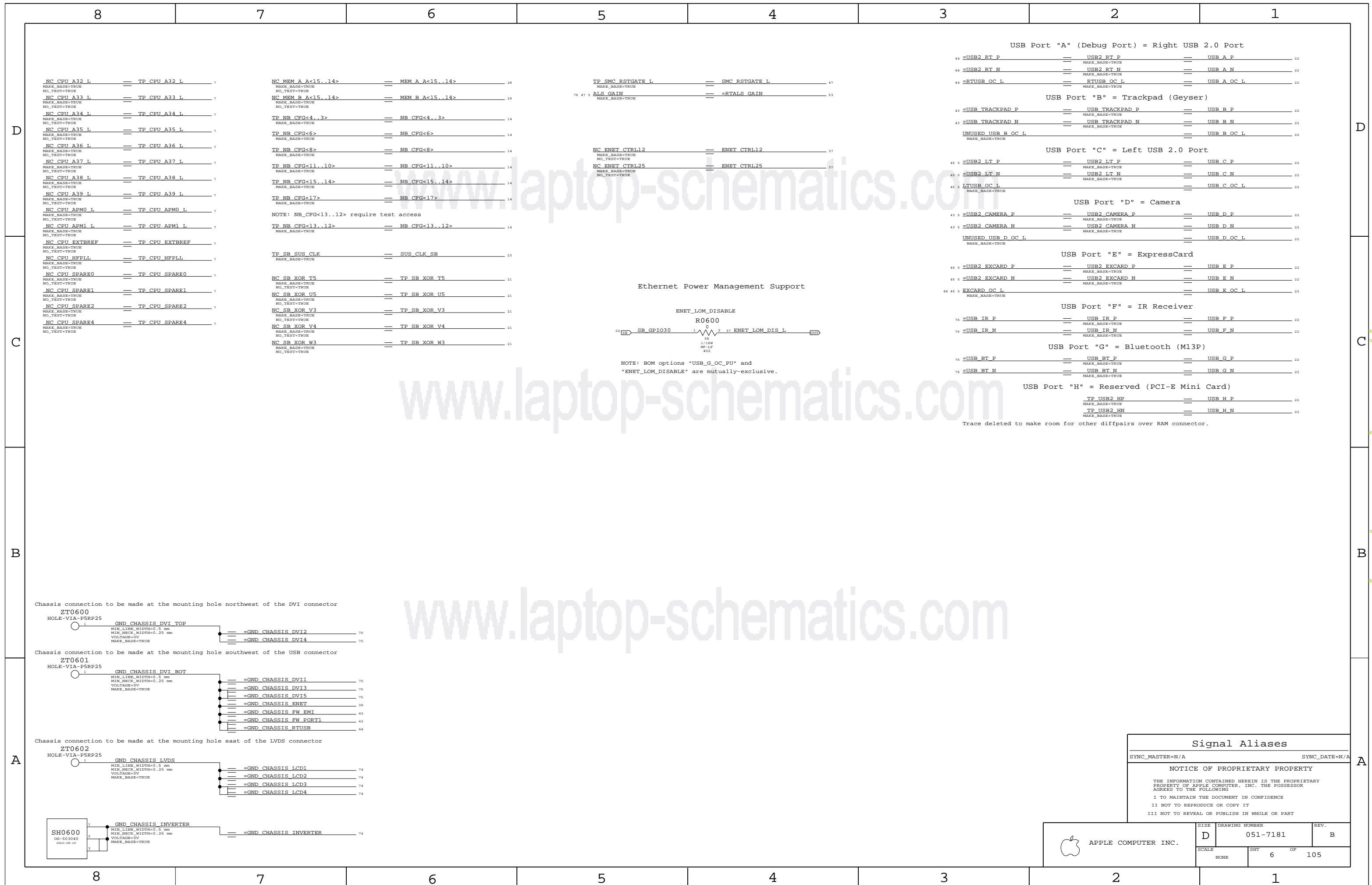
APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7181	REV. B
	SCALE NONE	SHT 2	OF 105



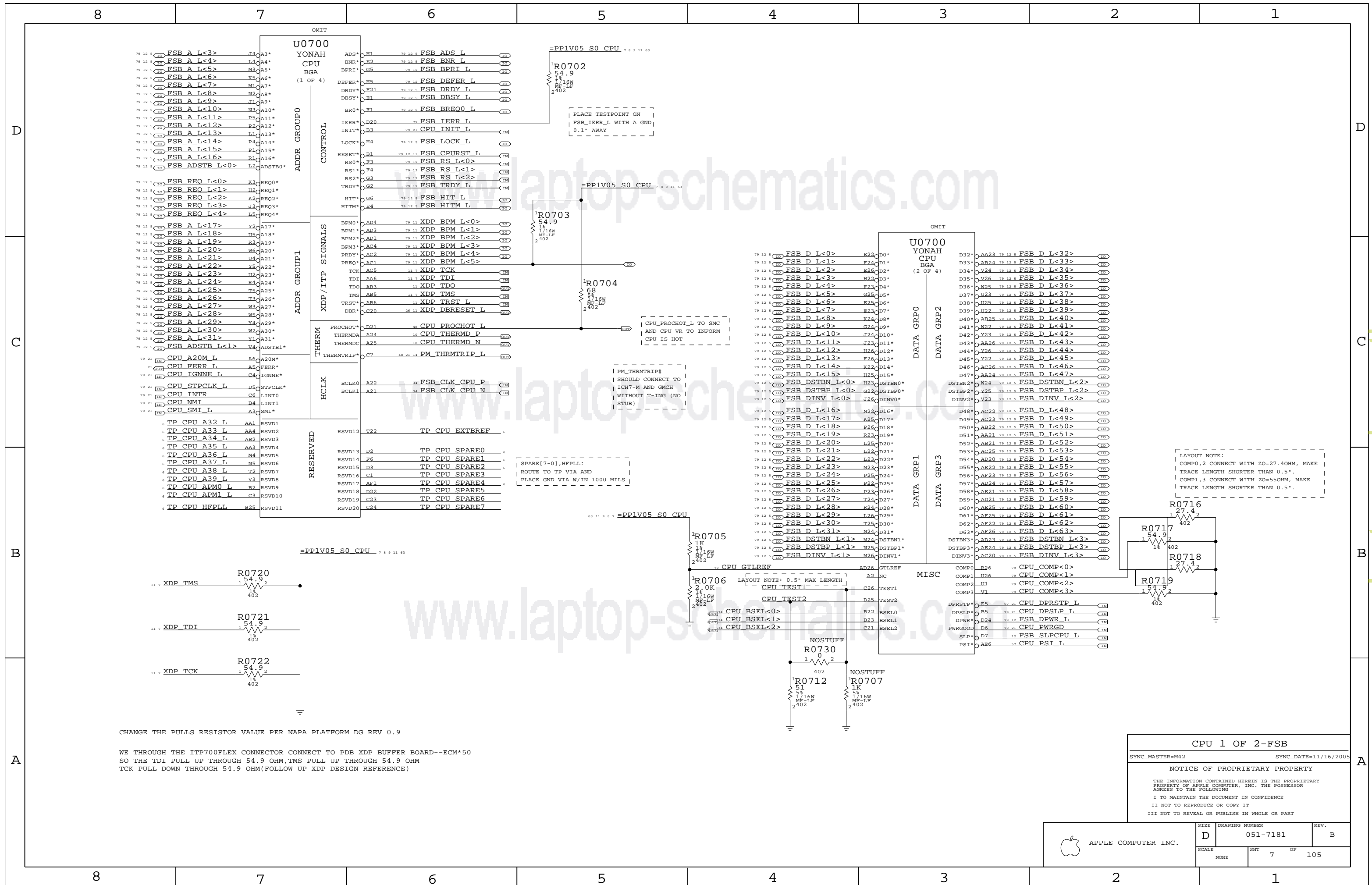
	8	7	6	5	4	3	2	1																																																																		
	BOMs																																																																									
	<table><tr><th>BOM NUMBER</th><th>BOM NAME</th><th>BOM OPTIONS</th></tr><tr><td>630-7754</td><td>PCBA, 2.16GHZ, 256VRAM, M1-RP_MBPPO_15</td><td>EEE_WB0, M1_COMMON, CPU_2_16GHZ, VRAM_SAM256</td></tr><tr><td>630-7756</td><td>PCBA, 2.0GHZ, 128VRAM, M1-RP_MBPPO_15</td><td>EEE_WB2, M1_COMMON, CPU_2_0GHZ, VRAM_SAM128</td></tr><tr><td>630-7757</td><td>PCBA, 2.0GHZ, 256VRAM, M1-RP_MBPPO_15</td><td>EEE_WB3, M1_COMMON, CPU_2_0GHZ, VRAM_SAM256</td></tr><tr><td>630-7760</td><td>PCBA, 1.83GHZ, 128VRAM, M1-RP_MBPPO_15</td><td>EEE_WB6, M1_COMMON, CPU_1_83GHZ, VRAM_SAM128</td></tr></table>								BOM NUMBER	BOM NAME	BOM OPTIONS	630-7754	PCBA, 2.16GHZ, 256VRAM, M1-RP_MBPPO_15	EEE_WB0, M1_COMMON, CPU_2_16GHZ, VRAM_SAM256	630-7756	PCBA, 2.0GHZ, 128VRAM, M1-RP_MBPPO_15	EEE_WB2, M1_COMMON, CPU_2_0GHZ, VRAM_SAM128	630-7757	PCBA, 2.0GHZ, 256VRAM, M1-RP_MBPPO_15	EEE_WB3, M1_COMMON, CPU_2_0GHZ, VRAM_SAM256	630-7760	PCBA, 1.83GHZ, 128VRAM, M1-RP_MBPPO_15	EEE_WB6, M1_COMMON, CPU_1_83GHZ, VRAM_SAM128																																																			
BOM NUMBER	BOM NAME	BOM OPTIONS																																																																								
630-7754	PCBA, 2.16GHZ, 256VRAM, M1-RP_MBPPO_15	EEE_WB0, M1_COMMON, CPU_2_16GHZ, VRAM_SAM256																																																																								
630-7756	PCBA, 2.0GHZ, 128VRAM, M1-RP_MBPPO_15	EEE_WB2, M1_COMMON, CPU_2_0GHZ, VRAM_SAM128																																																																								
630-7757	PCBA, 2.0GHZ, 256VRAM, M1-RP_MBPPO_15	EEE_WB3, M1_COMMON, CPU_2_0GHZ, VRAM_SAM256																																																																								
630-7760	PCBA, 1.83GHZ, 128VRAM, M1-RP_MBPPO_15	EEE_WB6, M1_COMMON, CPU_1_83GHZ, VRAM_SAM128																																																																								
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M1_COMMON2	HSTHMSNS_HAS, ITP, INVERTER_BUF, KBDLED_HAS, LPCPLUS, LVDS_PD, MEMVREF_S3																																																																									
M1_COMMON3	MEMVTT_EN_PU, RTUSB_ESD, SMC_PRGRM, USB_C_OC_PU, USB_D_OC_PU, USB_E_OC_PU																																																																									
VRAM_HY128	GPU_MEM_HYNIX, VRAM_128_HYNIX																																																																									
VRAM_SAM128	VRAM_128_SAMSUNG																																																																									
VRAM_HY256	GPU_MEM_256M, GPU_MEM_HYNIX, VRAM_256_HYNIX																																																																									
VRAM_SAM256	GPU_MEM_256M, VRAM_256_SAMSUNG																																																																									
	Bar Code Label / EEE #'s																																																																									
	<table><tr><th>PART NUMBER</th><th>QTY</th><th>DESCRIPTION</th><th>REFERENCE DES</th><th>CRITICAL</th><th>BOM OPTION</th></tr><tr><td>826-4393</td><td>1</td><td>LBL, P/N LABEL, PCB, 28MM X 6 MM</td><td>[EEE:WB6]</td><td>CRITICAL</td><td>EEE_WB6</td></tr><tr><td>826-4393</td><td>1</td><td>LBL, P/N LABEL, PCB, 28MM X 6 MM</td><td>[EEE:WB0]</td><td>CRITICAL</td><td>EEE_WB0</td></tr><tr><td>826-4393</td><td>1</td><td>LBL, P/N LABEL, PCB, 28MM X 6 MM</td><td>[EEE:WB2]</td><td>CRITICAL</td><td>EEE_WB2</td></tr><tr><td>826-4393</td><td>1</td><td>LBL, P/N LABEL, PCB, 28MM X 6 MM</td><td>[EEE:WB3]</td><td>CRITICAL</td><td>EEE_WB3</td></tr></table>								PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION	826-4393	1	LBL, P/N LABEL, PCB, 28MM X 6 MM	[EEE:WB6]	CRITICAL	EEE_WB6	826-4393	1	LBL, P/N LABEL, PCB, 28MM X 6 MM	[EEE:WB0]	CRITICAL	EEE_WB0	826-4393	1	LBL, P/N LABEL, PCB, 28MM X 6 MM	[EEE:WB2]	CRITICAL	EEE_WB2	826-4393	1	LBL, P/N LABEL, PCB, 28MM X 6 MM	[EEE:WB3]	CRITICAL	EEE_WB3																																				
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826-4393	1	LBL, P/N LABEL, PCB, 28MM X 6 MM	[EEE:WB2]	CRITICAL	EEE_WB2																																																																					
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PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION																																																																					
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333S0350	4	IC, SGRAM, GDDR3, 16MX32, 700MHZ, 136 FBGA	U8900, U8950, U9000, U9050	CRITICAL	VRAM_256_SAMSUNG																																																																					
333S0358	4	IC, SGRAM, GDDR3, 8MX32, 700MHZ, 136 FBGA	U8900, U8950, U9000, U9050	CRITICAL	VRAM_128_HYNIX																																																																					
333S0351	4	IC, SGRAM, GDDR3, 16MX32, 700MHZ, 136 FBGA	U8900, U8950, U9000, U9050	CRITICAL	VRAM_256_HYNIX																																																																					
337S3282	1	IC, YDC, CO, 1.83G, 31W, 667M, 2M, 479BGA	U0700	CRITICAL	CPU_1_83GHZ																																																																					
337S3267	1	IC, YDC, CO, 2.0G, 31W, 667M, 2M, 479BGA	U0700	CRITICAL	CPU_2_0GHZ																																																																					
337S3268	1	IC, YDC, CO, 2.16G, 31W, 667M, 2M, 479BGA	U0700	CRITICAL	CPU_2_16GHZ																																																																					
341S1934	1	IC, EFI, BOOTROM, V0055.03, MBPPO15	U6301	CRITICAL	BOOTROM_DEVEL																																																																					
338S0274	1	IC, SMC, HSB/2116	U5800	CRITICAL	SMC_BLANK																																																																					
341S1933	1	IC, PRGRM, SMC, V1.2F10 (M1) MBPPO15	U5800	CRITICAL	SMC_PRGRM																																																																					
	<table><tr><th>PART NUMBER</th><th>QTY</th><th>DESCRIPTION</th><th>REFERENCE DES</th><th>CRITICAL</th><th>BOM OPTION</th></tr><tr><td>338S0268</td><td>1</td><td>IC, FW32306, 1394A LINK, BGA, 129P</td><td>U4400</td><td>CRITICAL</td><td></td></tr><tr><td>338S0269</td><td>1</td><td>IC, 945GM, NORTHBRIDGE</td><td>U1200</td><td>CRITICAL</td><td></td></tr><tr><td>338S0270</td><td>1</td><td>IC, 8888053, GIGABIT ENET XCVR, 64P QFN, NO</td><td>U4101</td><td>CRITICAL</td><td></td></tr><tr><td>338S0309</td><td>1</td><td>IC, ATI, M56P, GRPHSCTRL, 880BGA, LP</td><td>U8400</td><td>CRITICAL</td><td>ATI_REV_B24</td></tr><tr><td>338S0315</td><td>1</td><td>IC, ATI, M56-LP, B26, GRPHXCTRL, LP 880BGA</td><td>U8400</td><td>CRITICAL</td><td>ATI_REV_B26</td></tr><tr><td>341S1789</td><td>1</td><td>IC, TPM, 28-PIN TSSOP</td><td>U6700</td><td>CRITICAL</td><td></td></tr><tr><td>341S1797</td><td>1</td><td>IC, EEPROM, SERIAL IIC, 8KBIT, SO8</td><td>U4102</td><td>CRITICAL</td><td></td></tr><tr><td>343S0385</td><td>1</td><td>IC, ICH7M, BGA</td><td>U2100</td><td>CRITICAL</td><td></td></tr><tr><td>353S1461</td><td>1</td><td>IC, ISL5904, SYNC REG CTRL, 2PHAS, QFN48, LP</td><td>U7530</td><td>CRITICAL</td><td></td></tr><tr><td>359S0101</td><td>1</td><td>IC, CY28445-5, CLOCK GEN, 68PIN QFN</td><td>U3301</td><td>CRITICAL</td><td></td></tr></table>								PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION	338S0268	1	IC, FW32306, 1394A LINK, BGA, 129P	U4400	CRITICAL		338S0269	1	IC, 945GM, NORTHBRIDGE	U1200	CRITICAL		338S0270	1	IC, 8888053, GIGABIT ENET XCVR, 64P QFN, NO	U4101	CRITICAL		338S0309	1	IC, ATI, M56P, GRPHSCTRL, 880BGA, LP	U8400	CRITICAL	ATI_REV_B24	338S0315	1	IC, ATI, M56-LP, B26, GRPHXCTRL, LP 880BGA	U8400	CRITICAL	ATI_REV_B26	341S1789	1	IC, TPM, 28-PIN TSSOP	U6700	CRITICAL		341S1797	1	IC, EEPROM, SERIAL IIC, 8KBIT, SO8	U4102	CRITICAL		343S0385	1	IC, ICH7M, BGA	U2100	CRITICAL		353S1461	1	IC, ISL5904, SYNC REG CTRL, 2PHAS, QFN48, LP	U7530	CRITICAL		359S0101	1	IC, CY28445-5, CLOCK GEN, 68PIN QFN	U3301	CRITICAL	
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	<table><tr><th>PART NUMBER</th><th>ALTERNATE FOR PART NUMBER</th><th>BOM OPTION</th><th>REF DES</th><th>COMMENTS:</th></tr><tr><td>128S0094</td><td>128S0060</td><td></td><td>ALL</td><td>330uF, 2V, 9M0HM, D2</td></tr><tr><td>128S0095</td><td>128S0060</td><td></td><td>ALL</td><td>330uF, 2V, 6M0HM, D2</td></tr><tr><td>128S0081</td><td>128S0061</td><td></td><td>ALL</td><td>150uF, 6.3V, 25M0HM, C2</td></tr><tr><td>128S0077</td><td>128S0086</td><td></td><td>ALL</td><td>7m0hm alt for 8m0hm</td></tr></table>								PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:	128S0094	128S0060		ALL	330uF, 2V, 9M0HM, D2	128S0095	128S0060		ALL	330uF, 2V, 6M0HM, D2	128S0081	128S0061		ALL	150uF, 6.3V, 25M0HM, C2	128S0077	128S0086		ALL	7m0hm alt for 8m0hm																																									
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	<div><div><div><div><div><div></div><div>APPLE COMPUTER INC.</div></div></div><div><div>SIZE</div><div>D</div></div><div><div>SCALE</div><div>NONE</div></div></div><div><div>DRAWING NUMBER</div><div>051-7181</div></div><div><div>SHT</div><div>4</div><div>OF</div><div>105</div></div><div><div>REV.</div><div>B</div></div></div><div><div><div>BOM Configuration</div><div>SYNC_MASTER=N/A</div><div>SYNC_DATE=N/A</div><div>NOTICE OF PROPRIETARY PROPERTY</div><div>THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING</div><div>I TO MAINTAIN THE DOCUMENT IN CONFIDENCE</div><div>II NOT TO REPRODUCE OR COPY IT</div><div>III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART</div></div></div></div>																																																																									
	8	7	6	5	4	3	2	1																																																																		

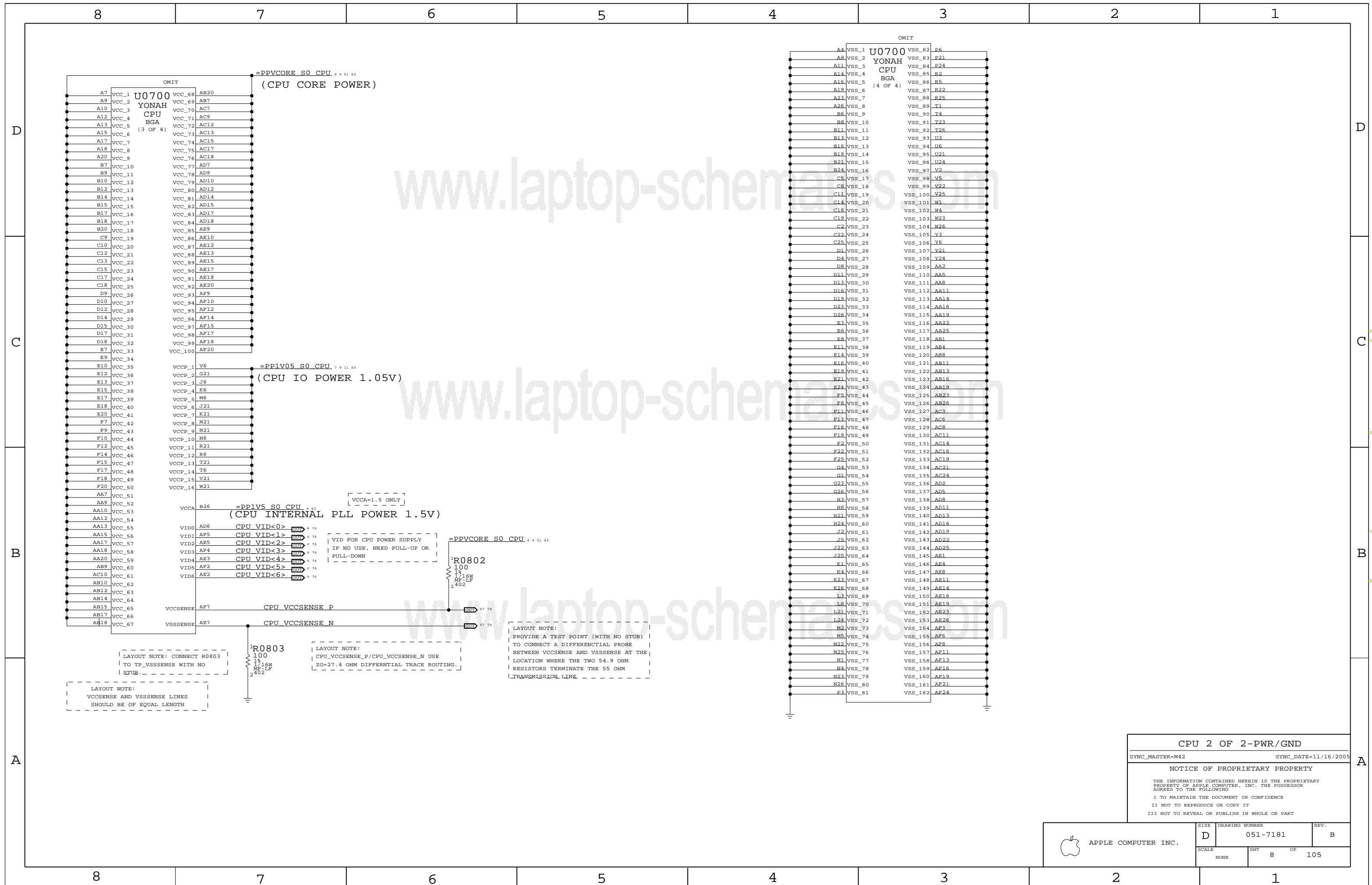
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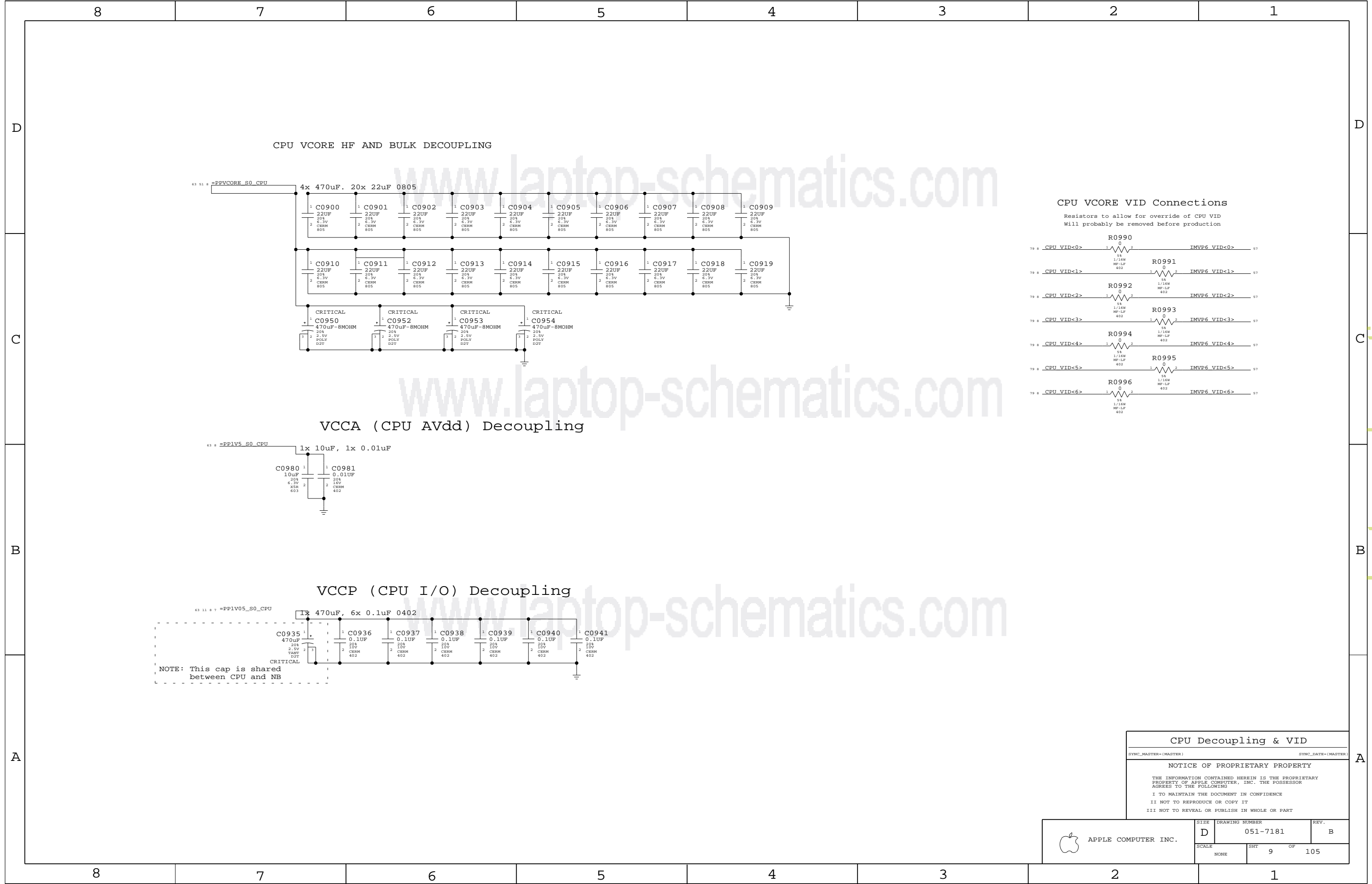


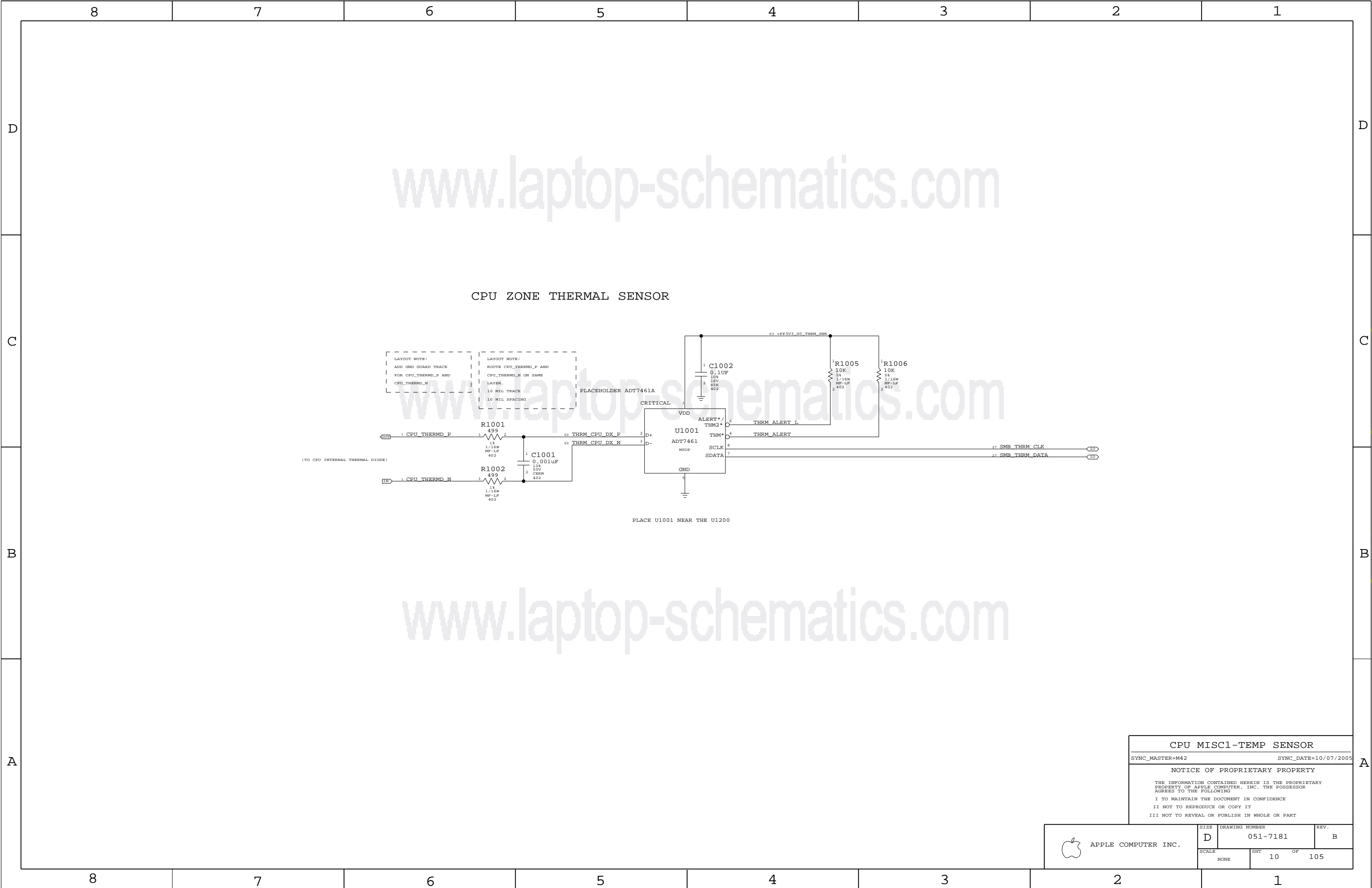










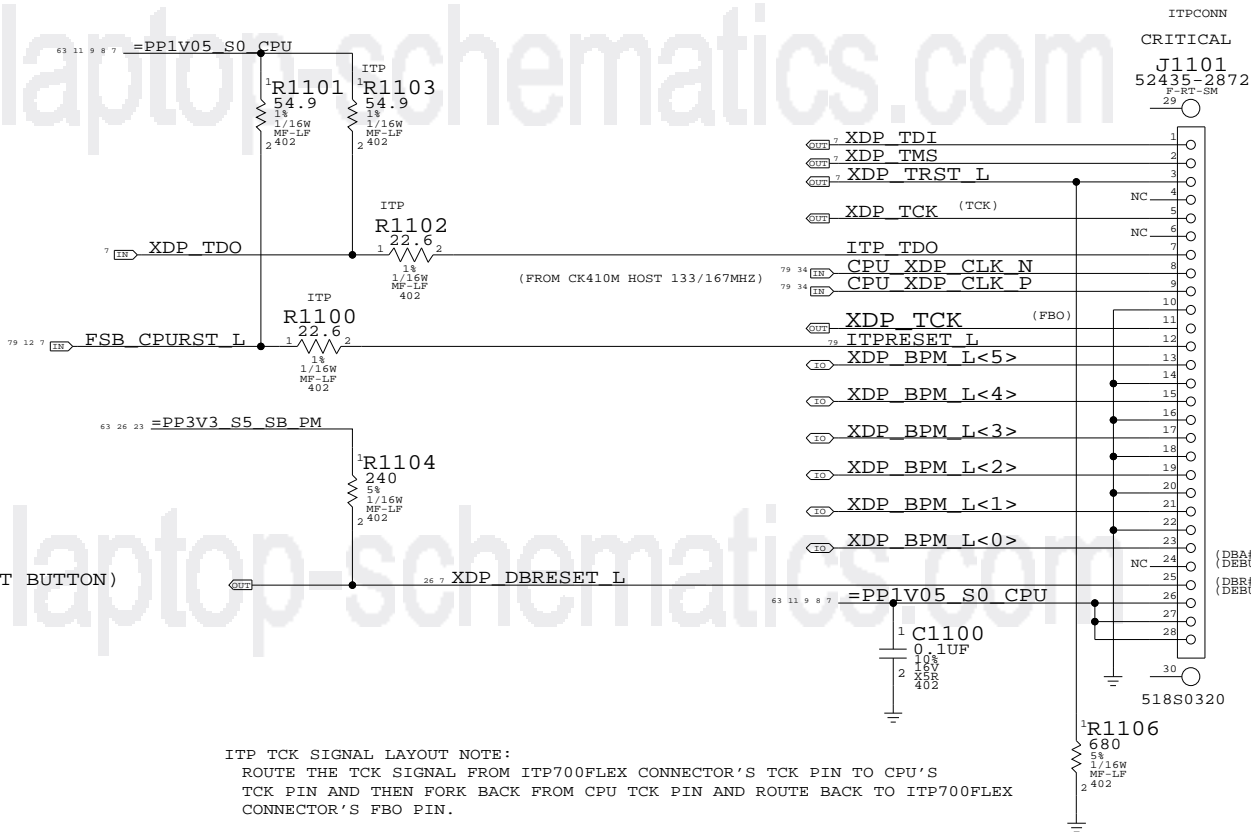


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CPU ITP700FLEX DEBUG SUPPORT

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ITP TCK SIGNAL LAYOUT NOTE:  
ROUTE THE TCK SIGNAL FROM ITP700FLEX CONNECTOR'S TCK PIN TO CPU'S  
TCK PIN AND THEN FORK BACK FROM CPU TCK PIN AND ROUTE BACK TO ITP700FLEX  
CONNECTOR'S FBO PIN.



APPLE COMPUTER INC.

CPU ITP700FLEX DEBUG

SYNC\_MASTER=M42 SYNC\_DATE=10/12/2005

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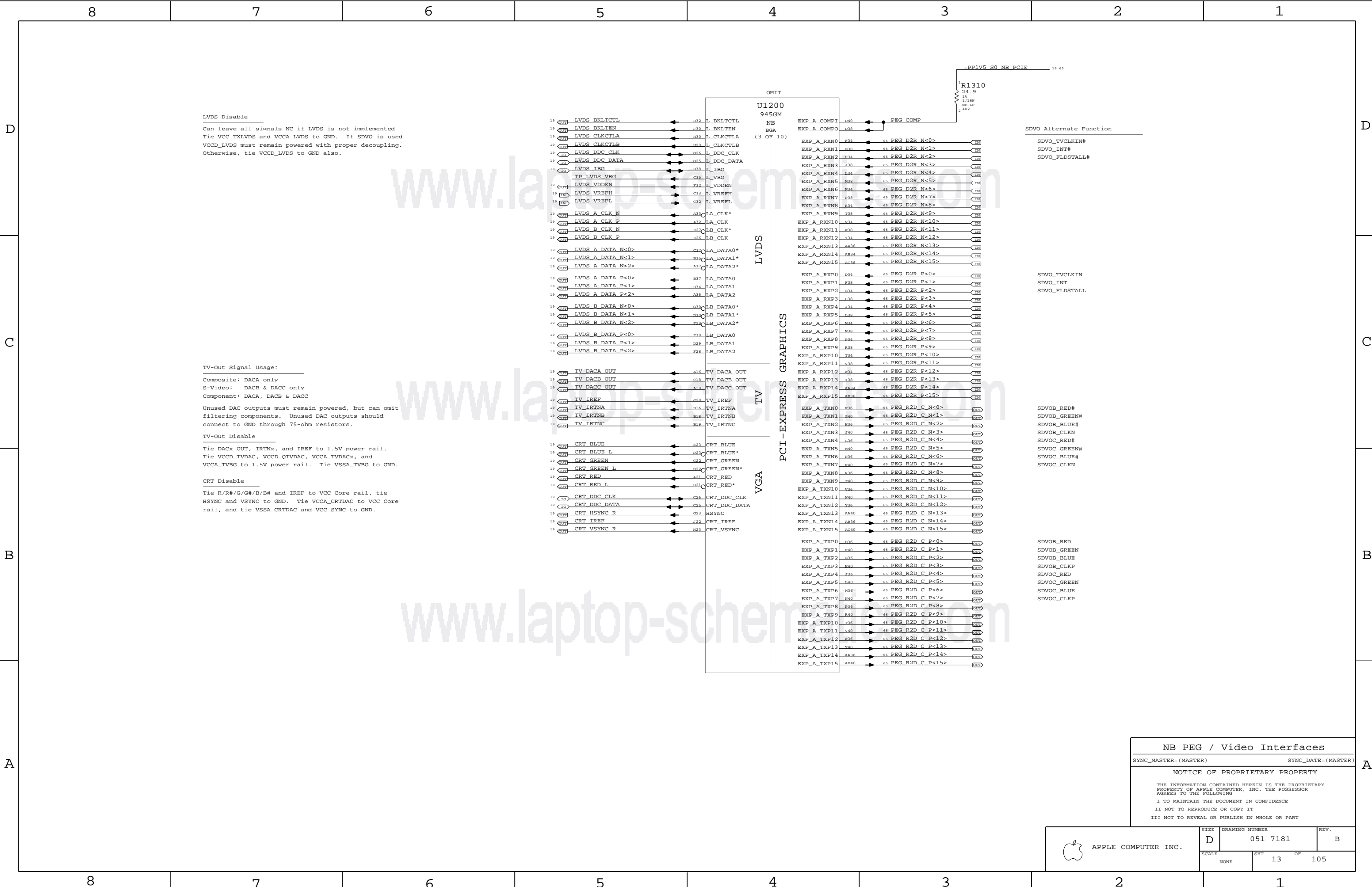
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SIZE D DRAWING NUMBER 051-7181 REV. B

SCALE NONE SHT 11 OF 105





**LVDS Disable**

Can leave all signals NC if LVDS is not implemented  
Tie VCC\_TXLVDS and VCCA\_LVDS to GND. If SDVO is used  
VCCD\_LVDS must remain powered with proper decoupling.  
Otherwise, tie VCCD\_LVDS to GND also.

**TV-Out Signal Usage:**

Composite: DACA only  
S-Video: DACB & DACC only  
Component: DACA, DACB & DACC

Unused DAC outputs must remain powered, but can omit  
filtering components. Unused DAC outputs should  
connect to GND through 75-ohm resistors.

**TV-Out Disable**

Tie DACx\_OUT, IRTNx, and IREF to 1.5V power rail.  
Tie VCCD\_TVDAC, VCCD\_QTVDAC, VCCA\_TVDACx, and  
VCCA\_TVBG to 1.5V power rail. Tie VSSA\_TVBG to GND.

**CRT Disable**

Tie R/R#/G/G#/B/B# and IREF to VCC Core rail, tie  
HSYNC and VSYNC to GND. Tie VCCA\_CRTDAC to VCC Core  
rail, and tie VSSA\_CRTDAC and VCC\_SYNC to GND.

NB PEG / Video Interfaces

SYNC\_MASTER=(MASTER)

SYNC\_DATE=(MASTER)

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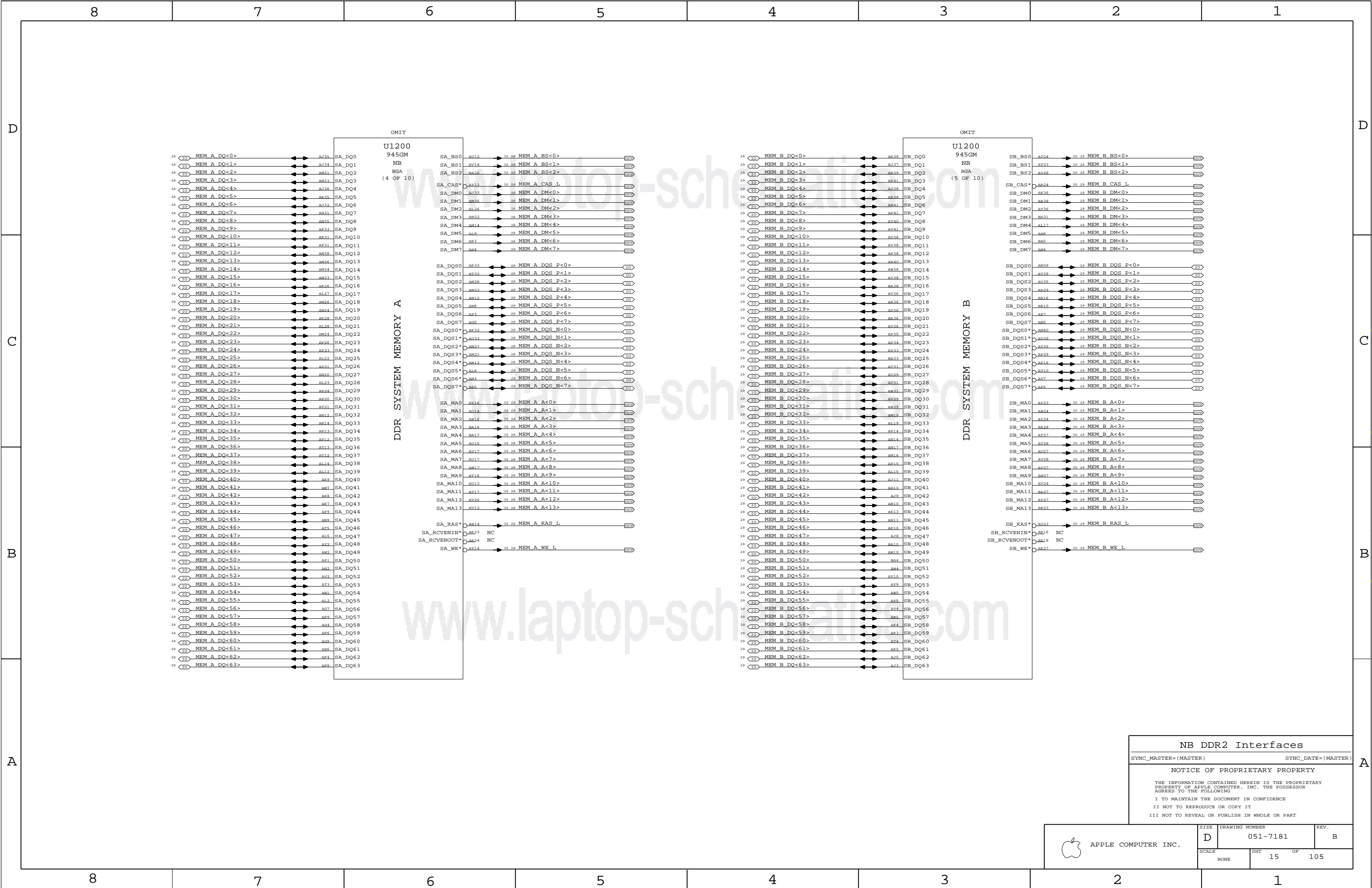
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 APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7181	REV. B
	SCALE NONE	SHT 13	OF 105







NB DDR2 Interfaces

SYNC\_MASTER=(MASTER) SYNC\_DATE=(MASTER)

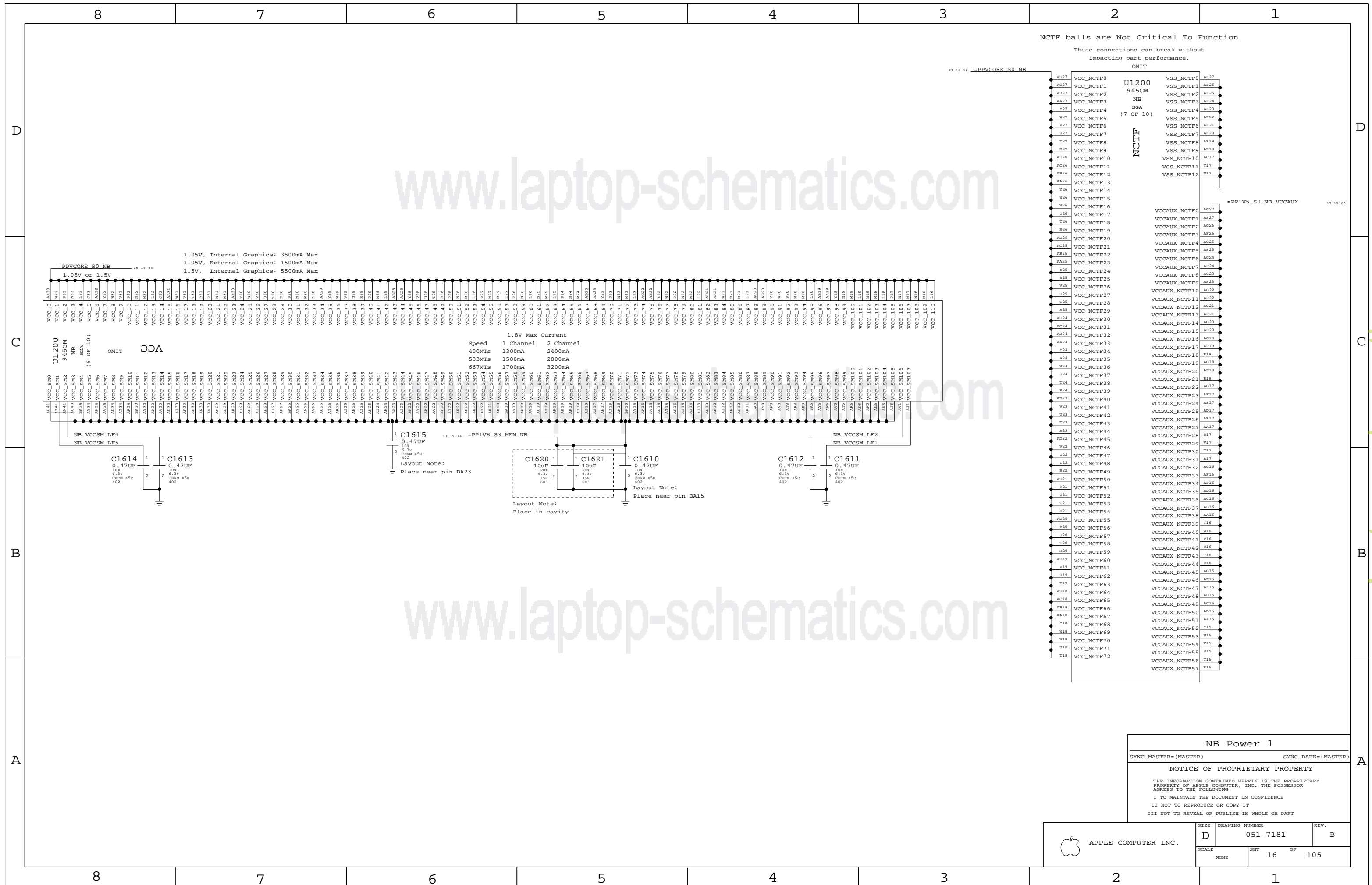
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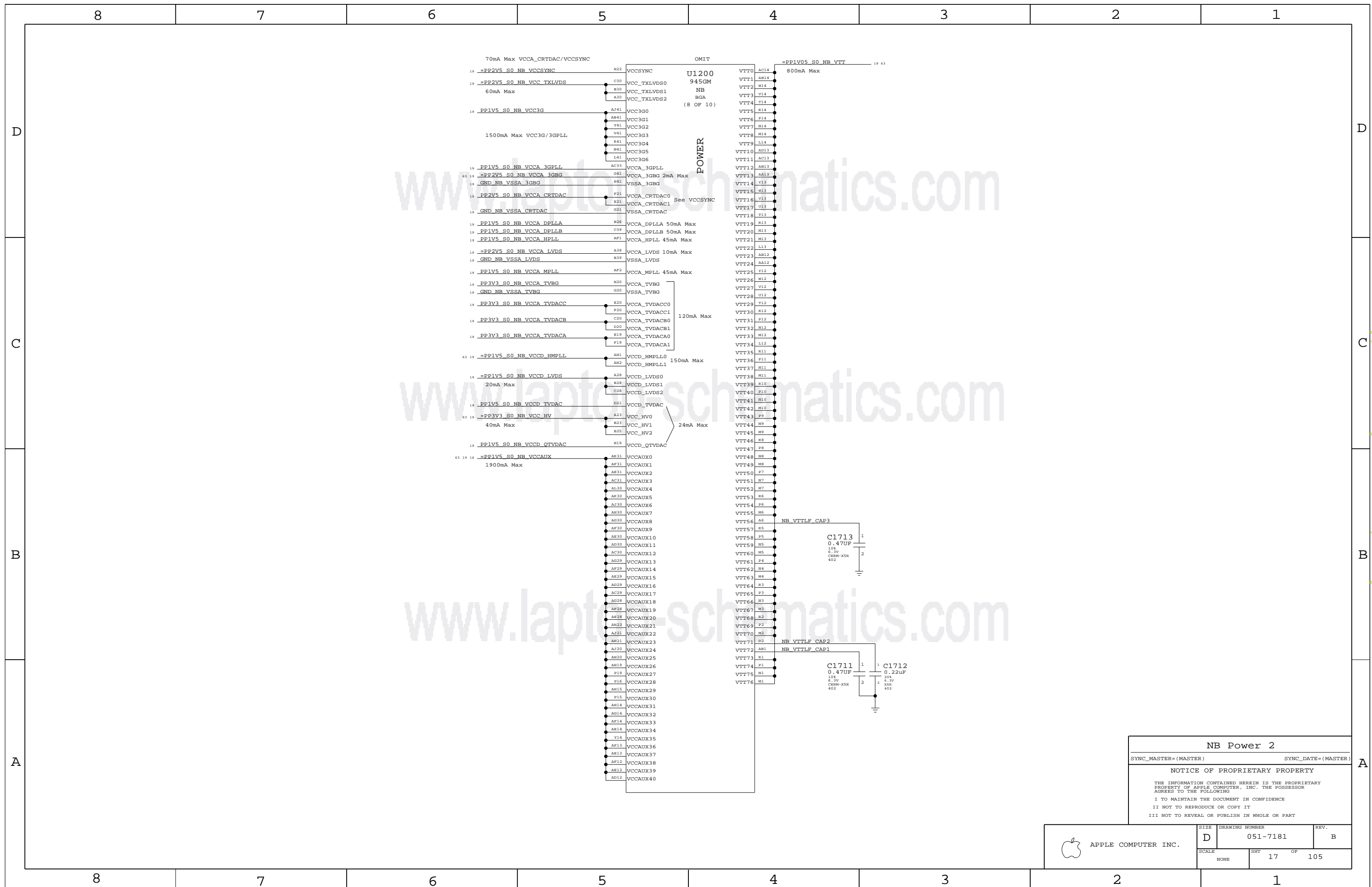
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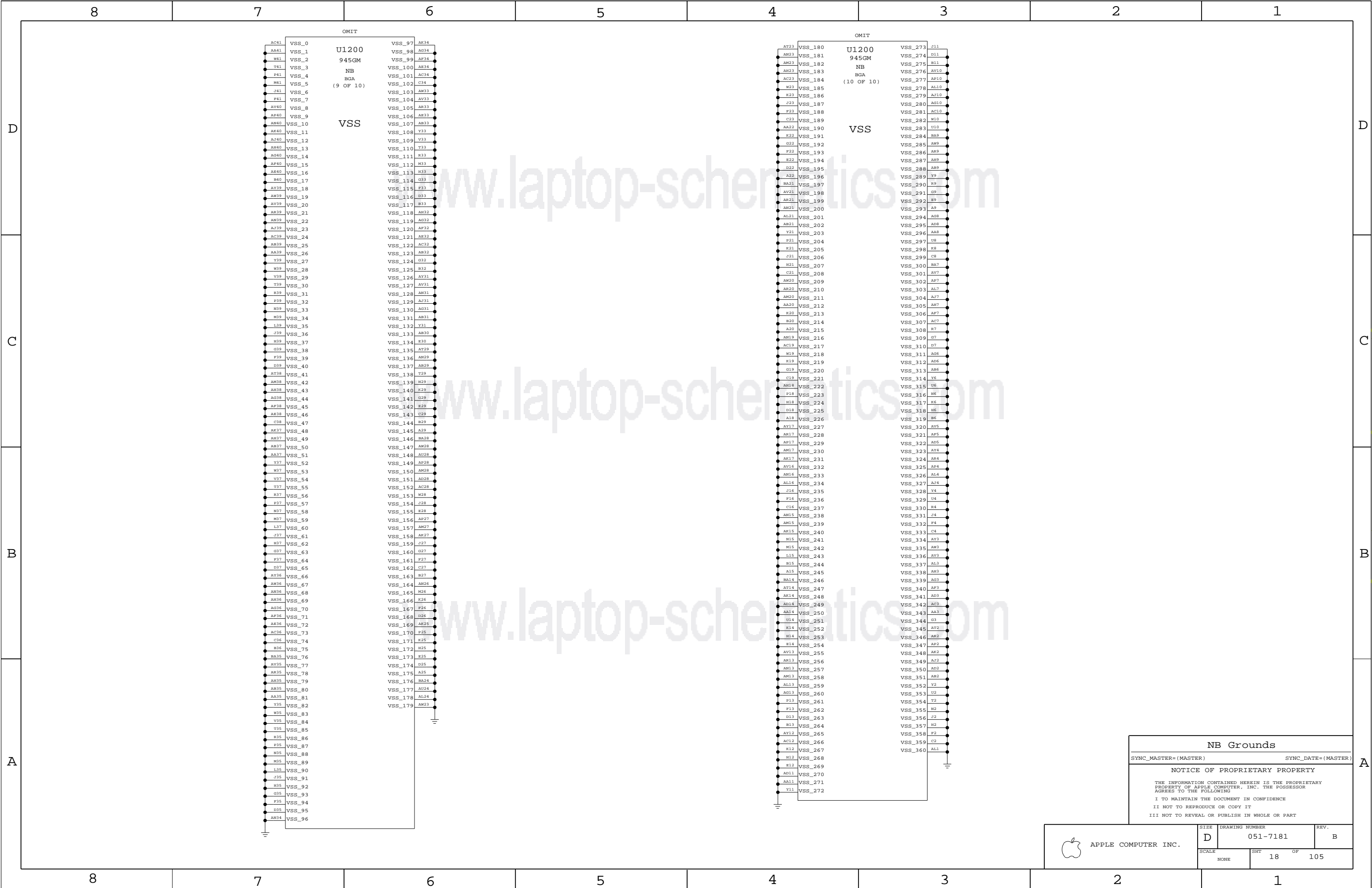
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NB Grounds

SYNC\_MASTER=(MASTER) SYNC\_DATE=(MASTER)

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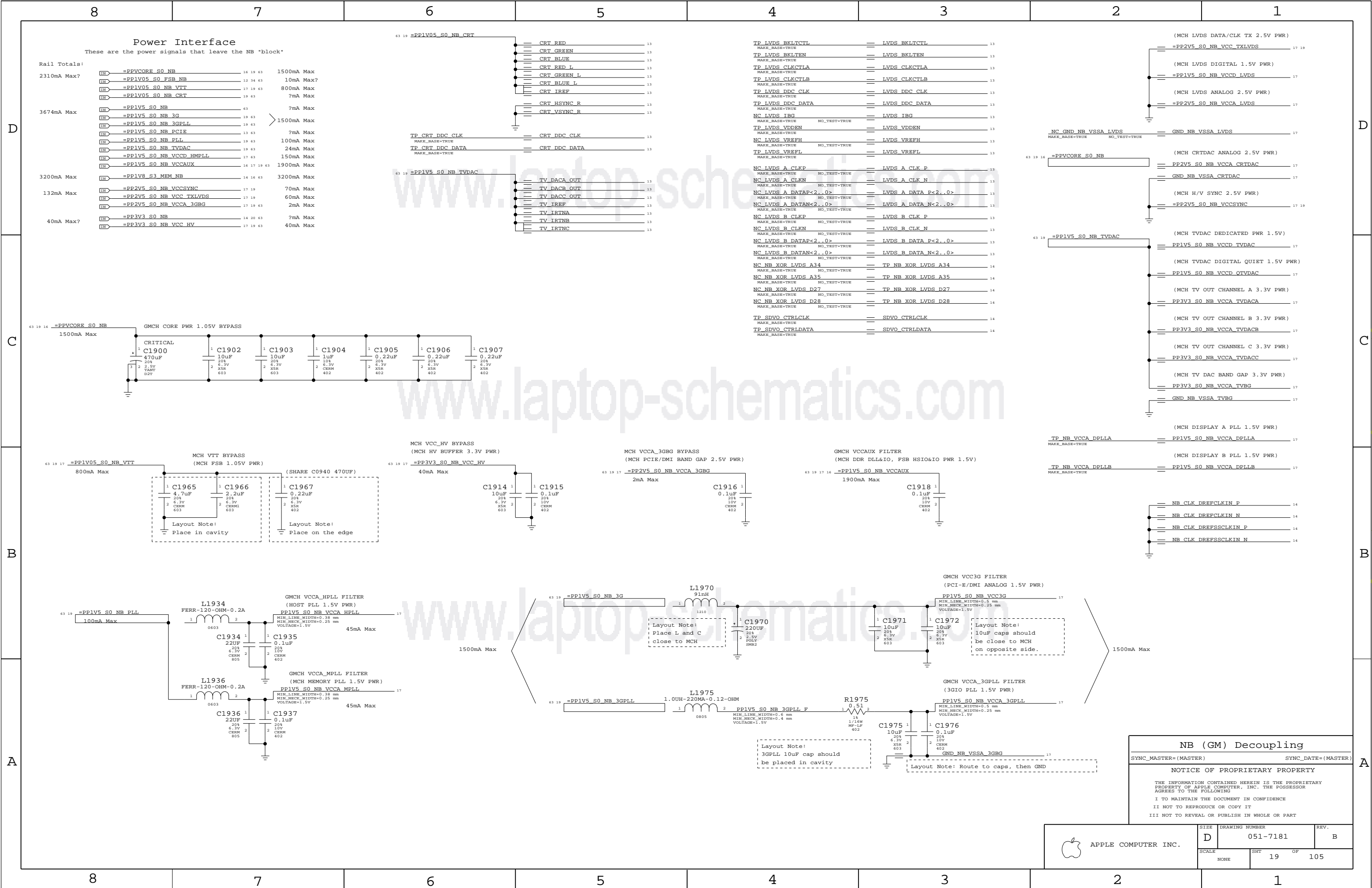
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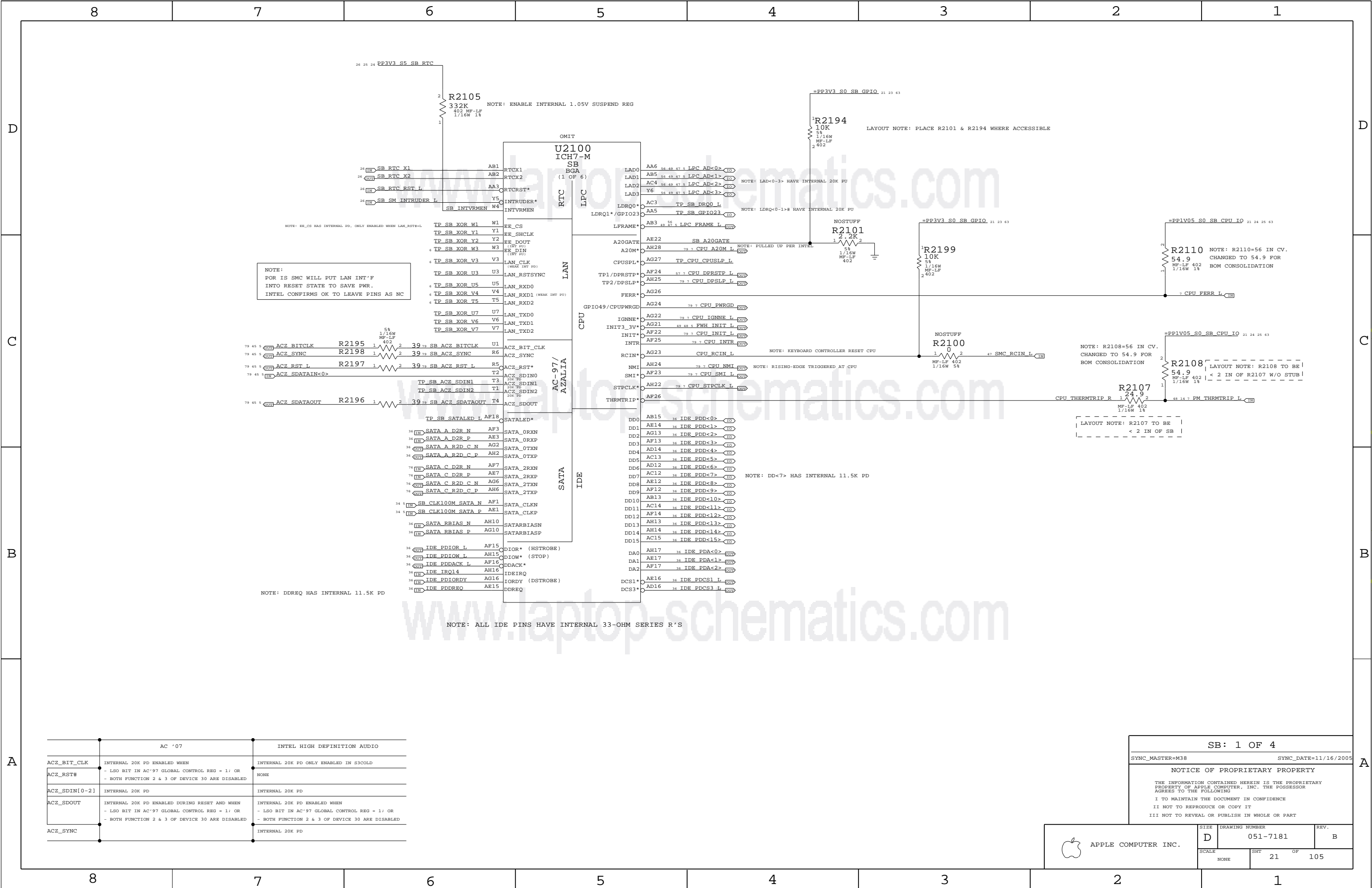
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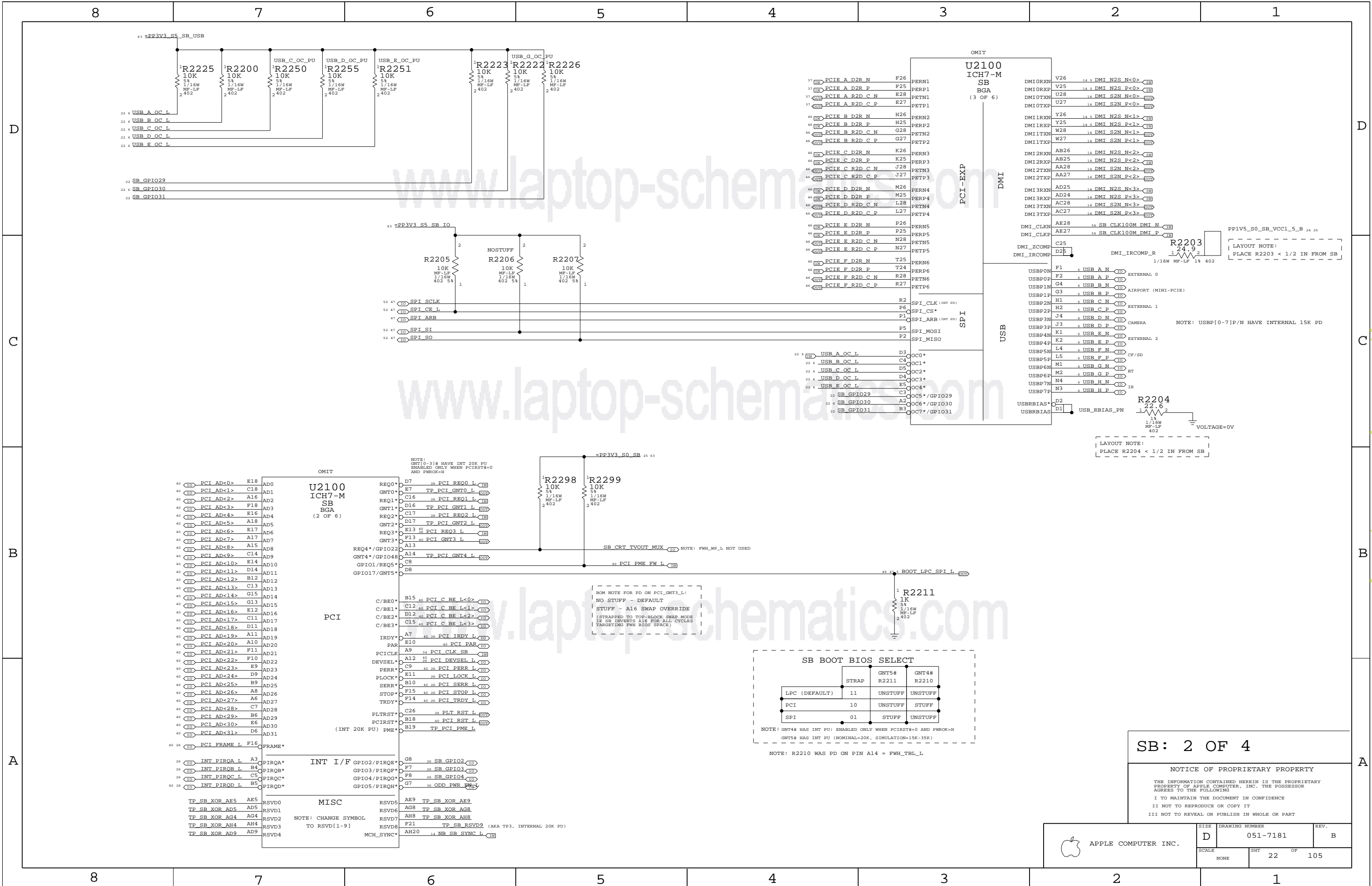
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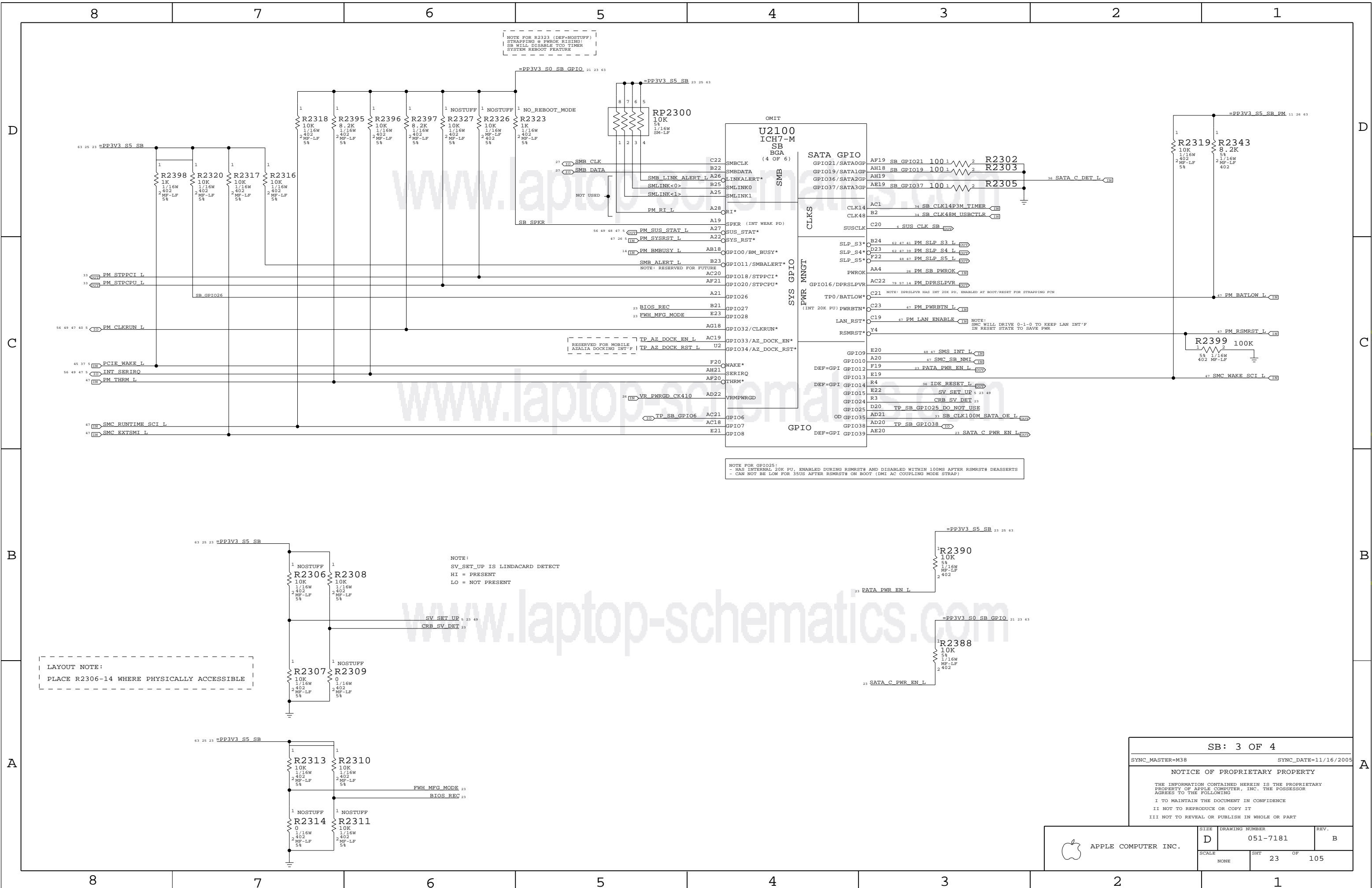












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SB: 3 OF 4

SYNC\_MASTER=M38

SYNC\_DATE=11/16/2005

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SIZE D

DRAWING NUMBER 051-7181

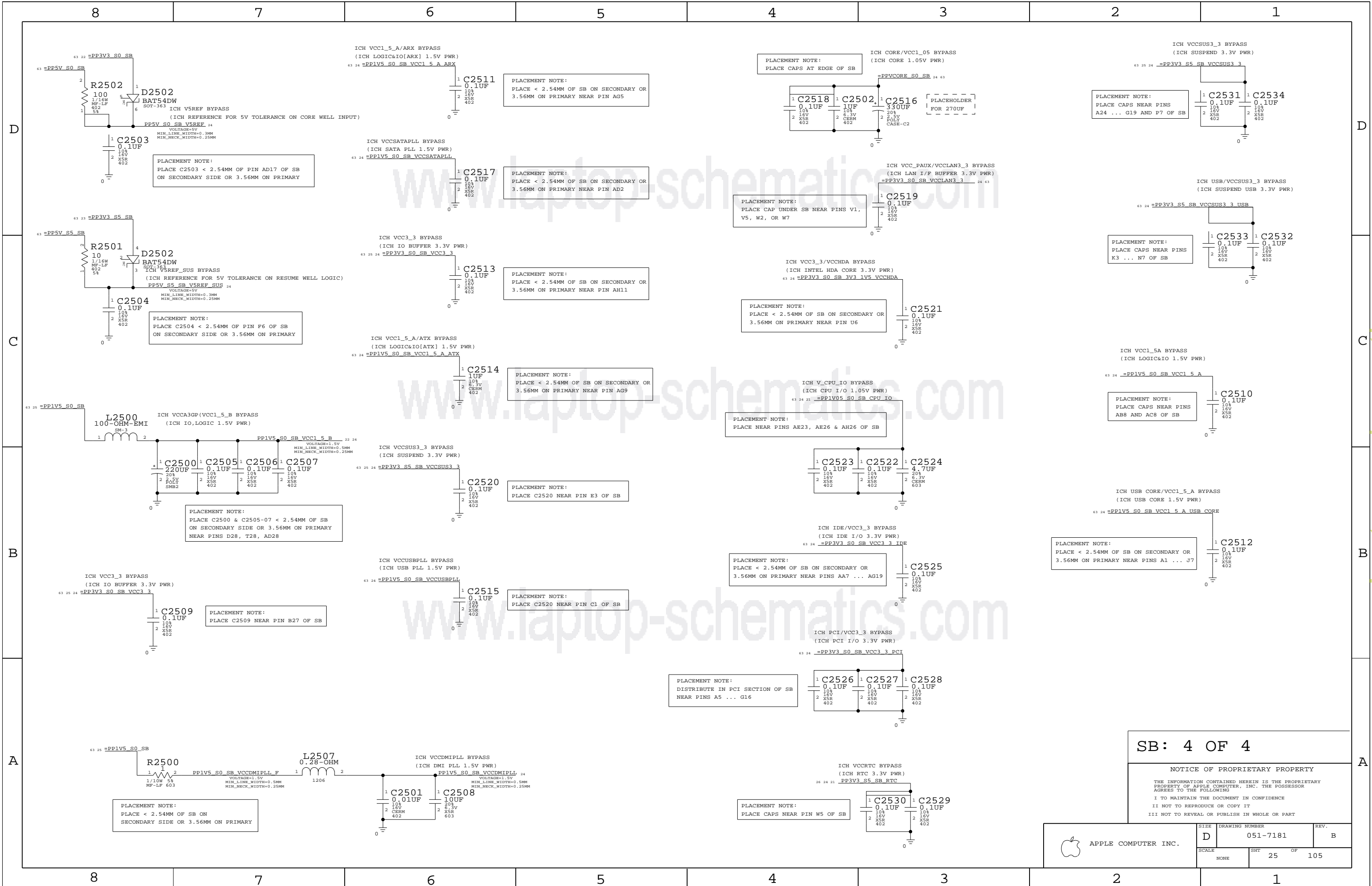
REV. B

SCALE NONE

SHT 23 OF 105







SB: 4 OF 4

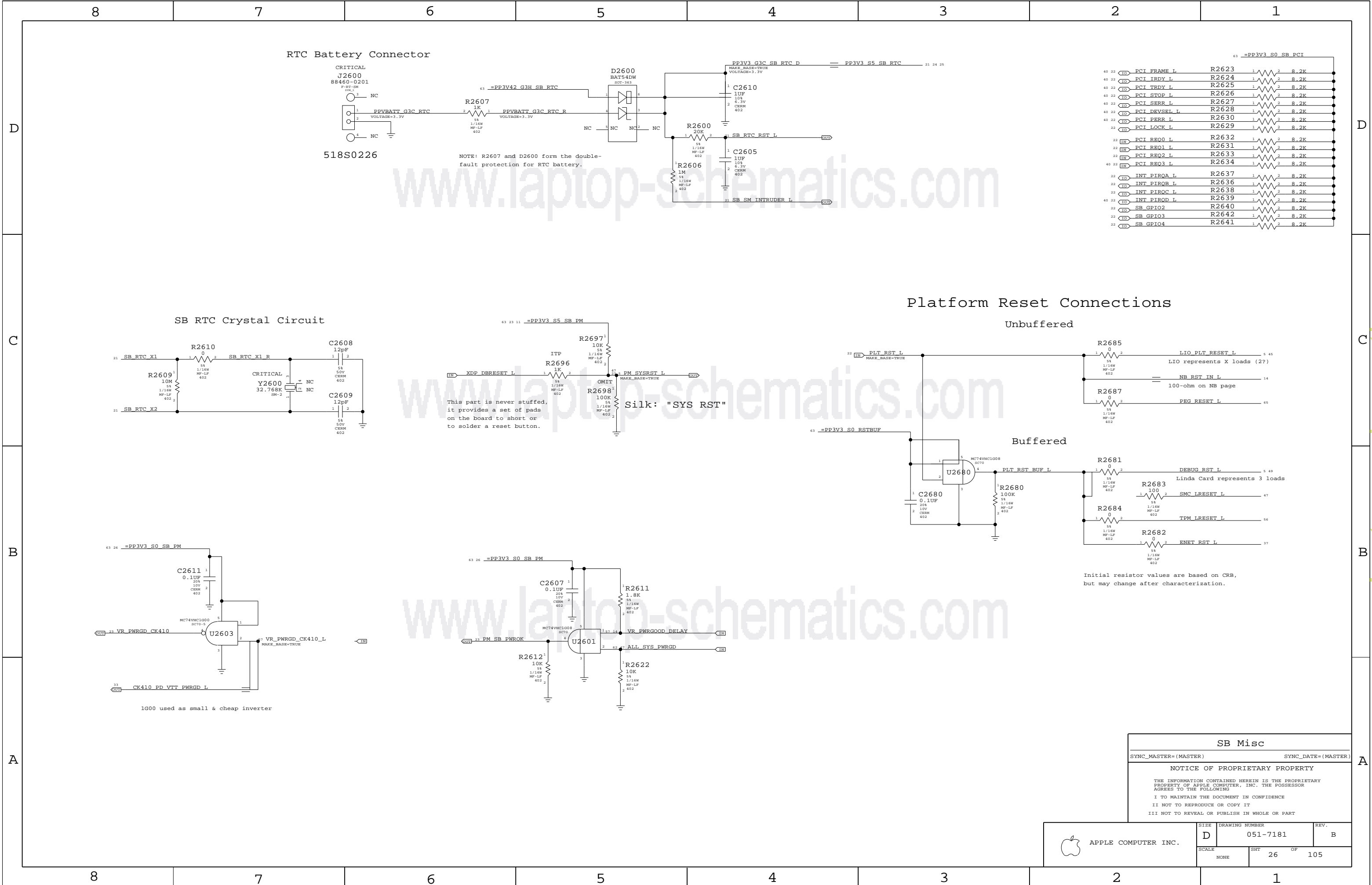
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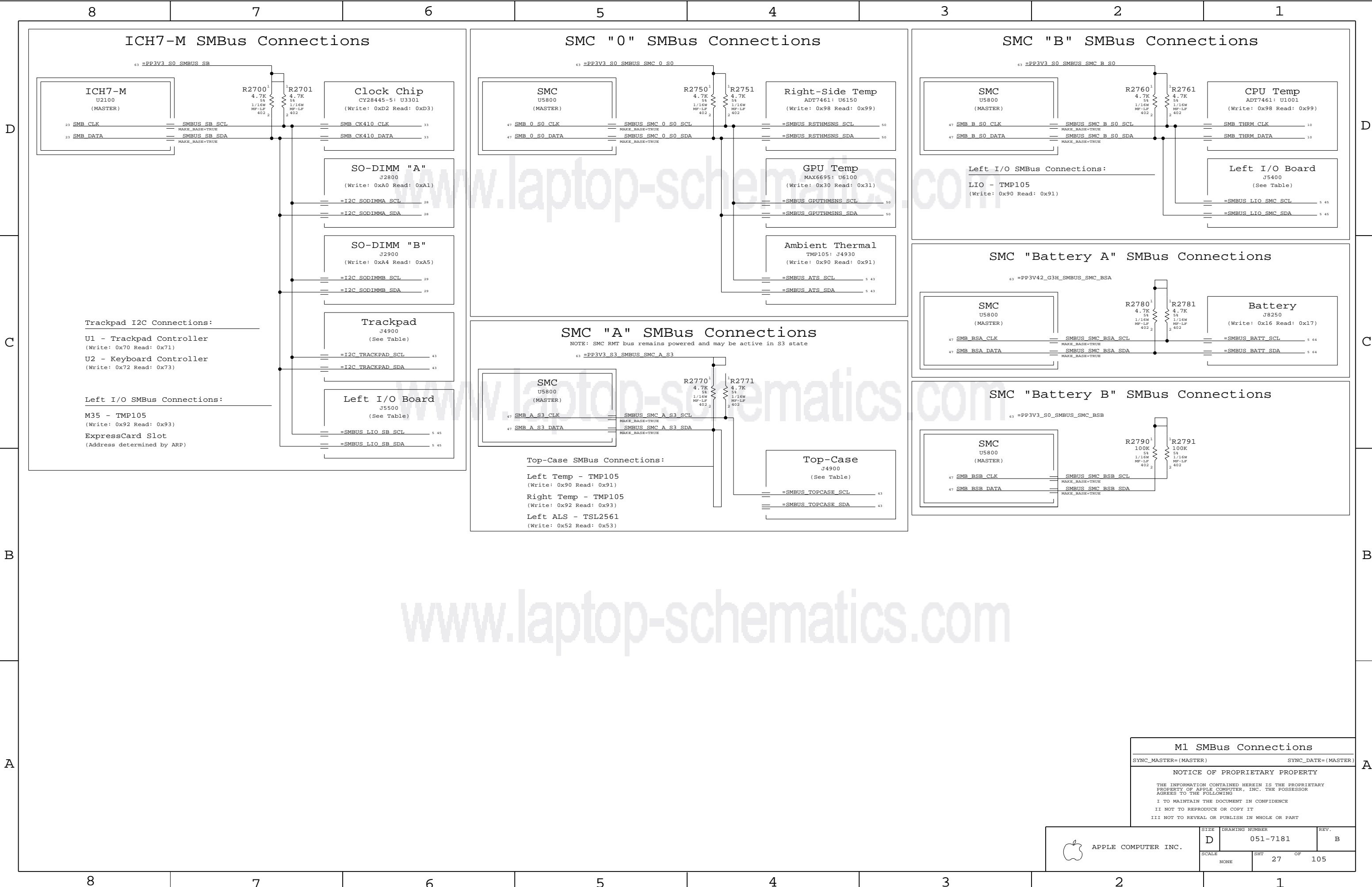
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SIZE	DRAWING NUMBER	REV.
D	051-7181	B
SCALE	SHT	OF
NONE	25	105





M1 SMBus Connections

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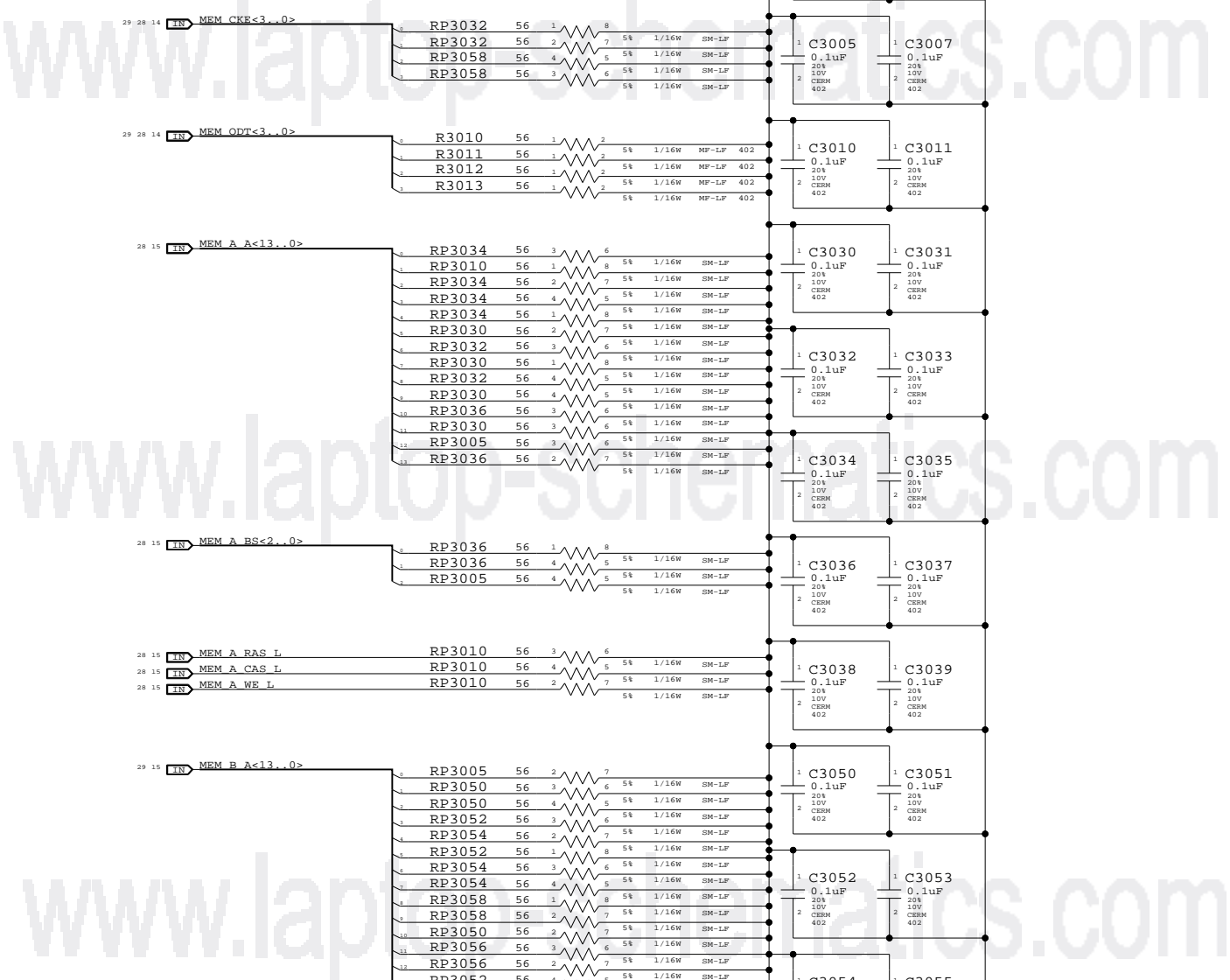
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-7181	B
SCALE		SHT	OF
NONE		27	105









Power aliases required by this page:

- PP5V\_S0\_MEMVTT
- PP1V8\_S0\_MEMVTT
- PP0V9\_S0\_MEMVTT\_LDO

---

Signal aliases required by this page:

(NONE)

---

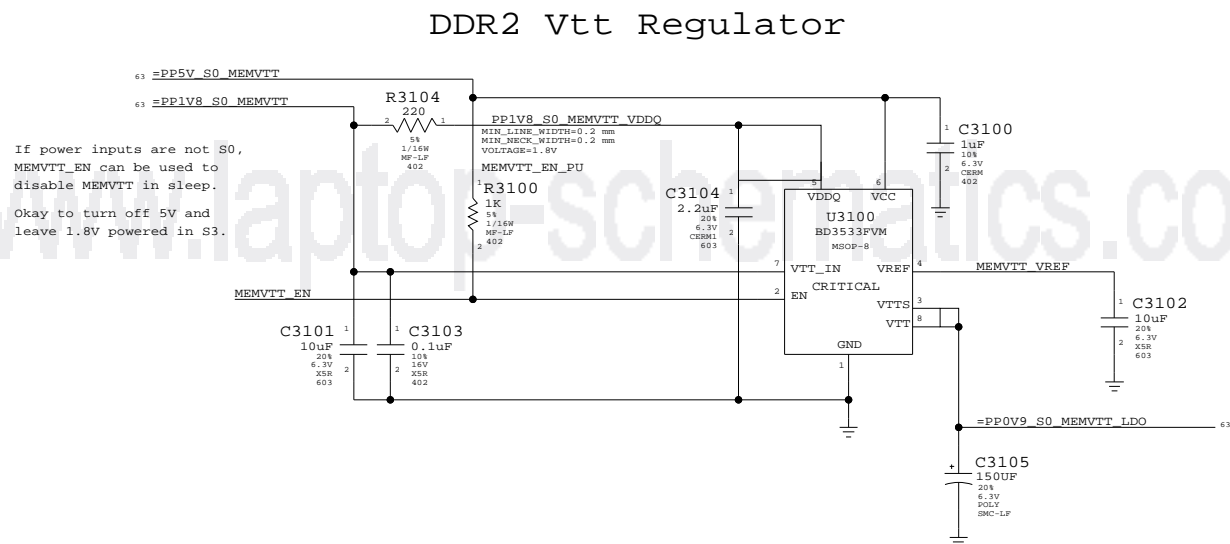
BOM options provided by this page:

(NONE)

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- =PP5V_S0_MEMVTT
- =PP1V8_S0_MEMVTT
- =PP0V9_S0_MEMVTT_LDO
```

( NONE )

( NONE )



If power inputs are not S0, MEMVTT\_EN can be used to disable MEMVTT in sleep.

Okay to turn off 5V and leave 1.8V powered in S3.

```

Memory Vtt Supply
-----
SYNC_MASTER=(MASTER)                                SYNC_DATE=(MASTER)
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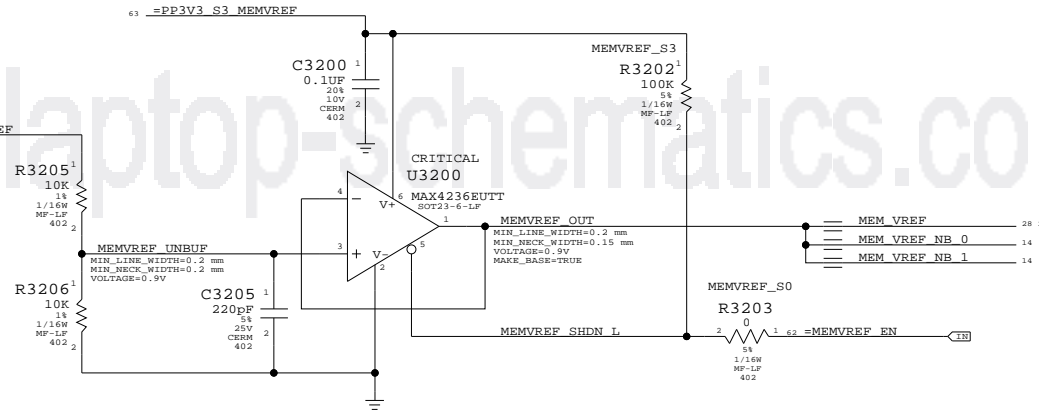
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SIZE D	DRAWING NUMBER 051-7181	REV. B
SCALE NONE	SHT 31	OF 105

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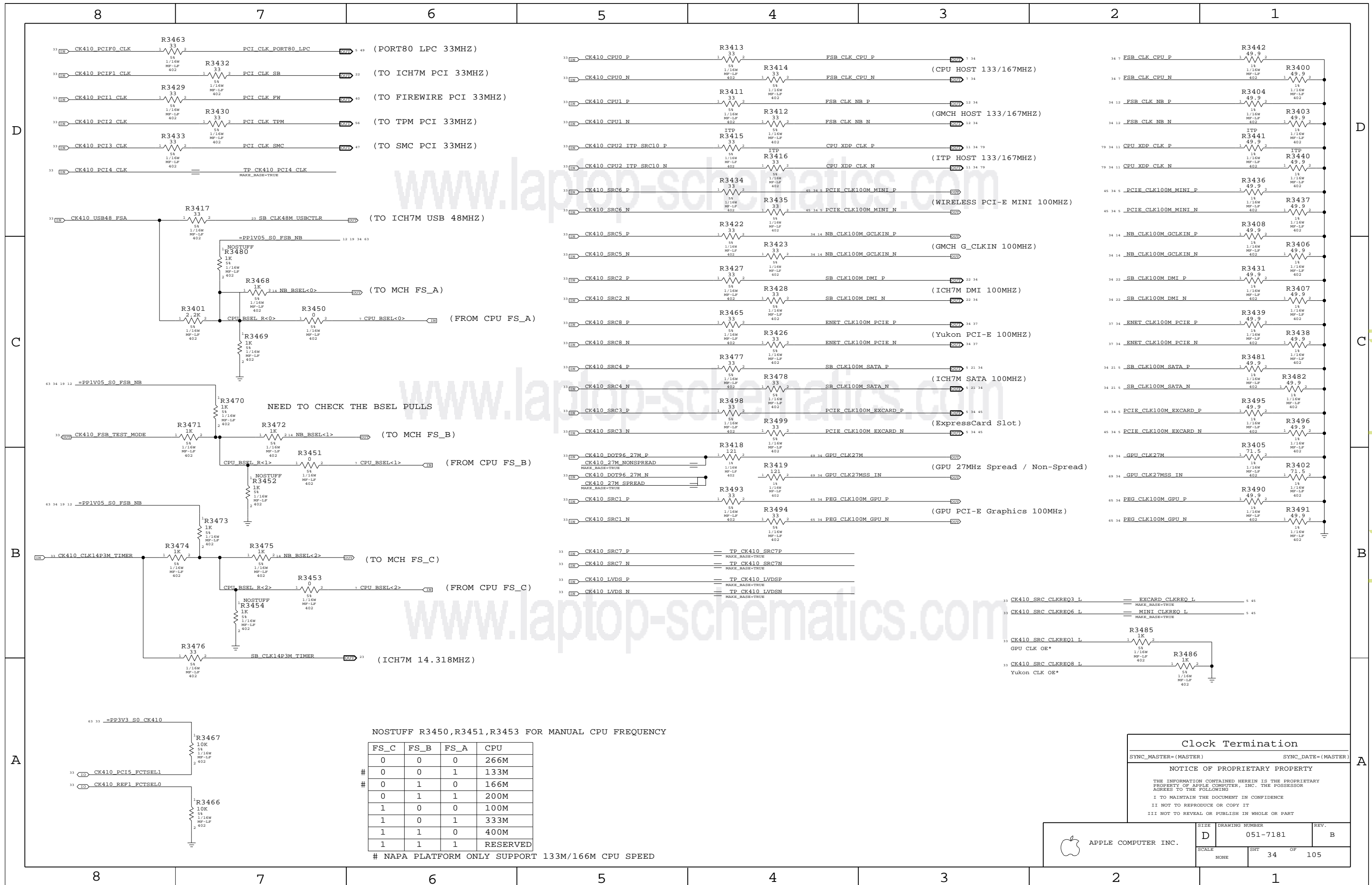
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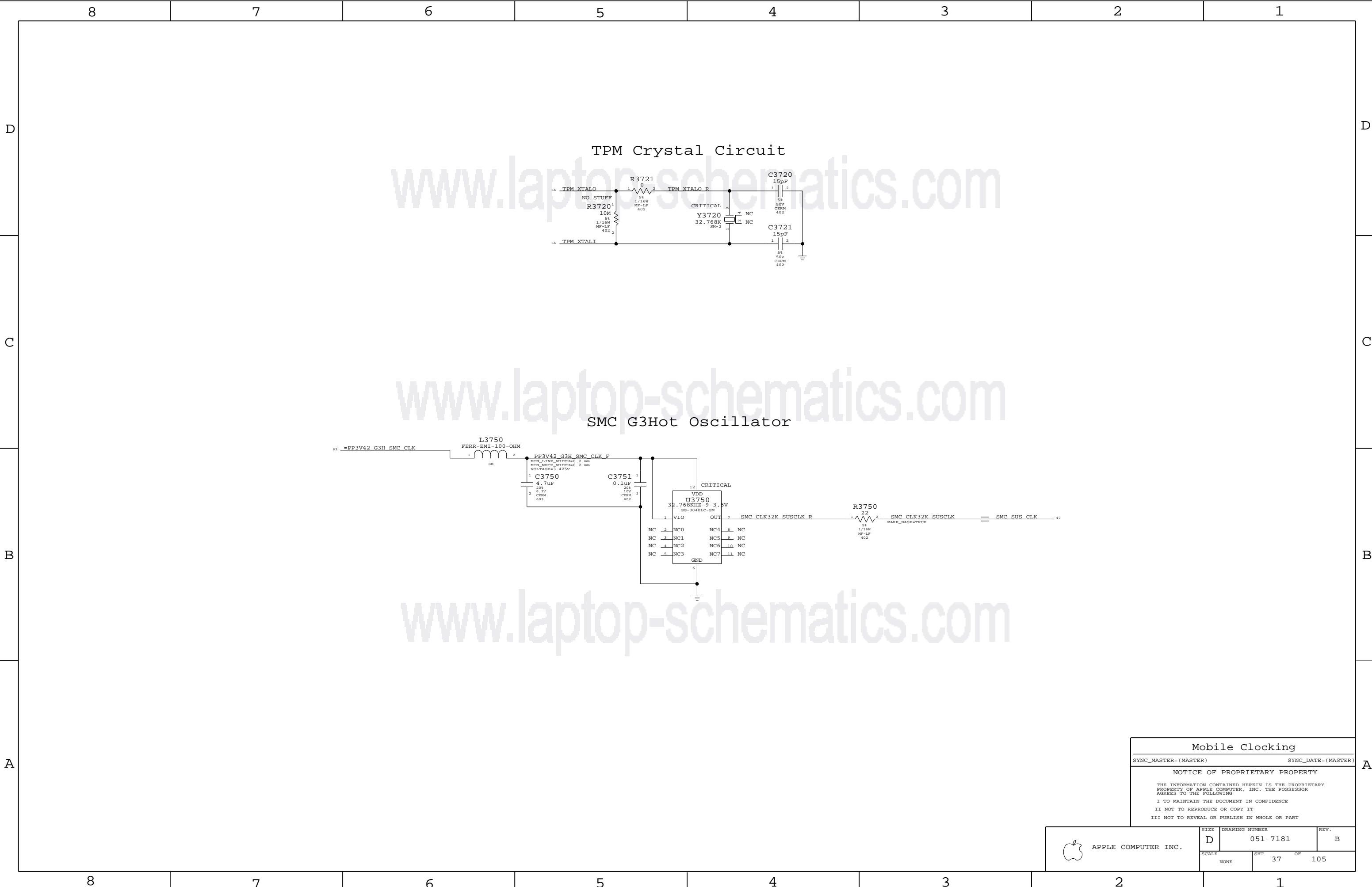
DDR2 VRef	
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	SCALE NONE	SHT 32	OF 105









Mobile Clocking

SYNC\_MASTER=(MASTER) SYNC\_DATE=(MASTER)

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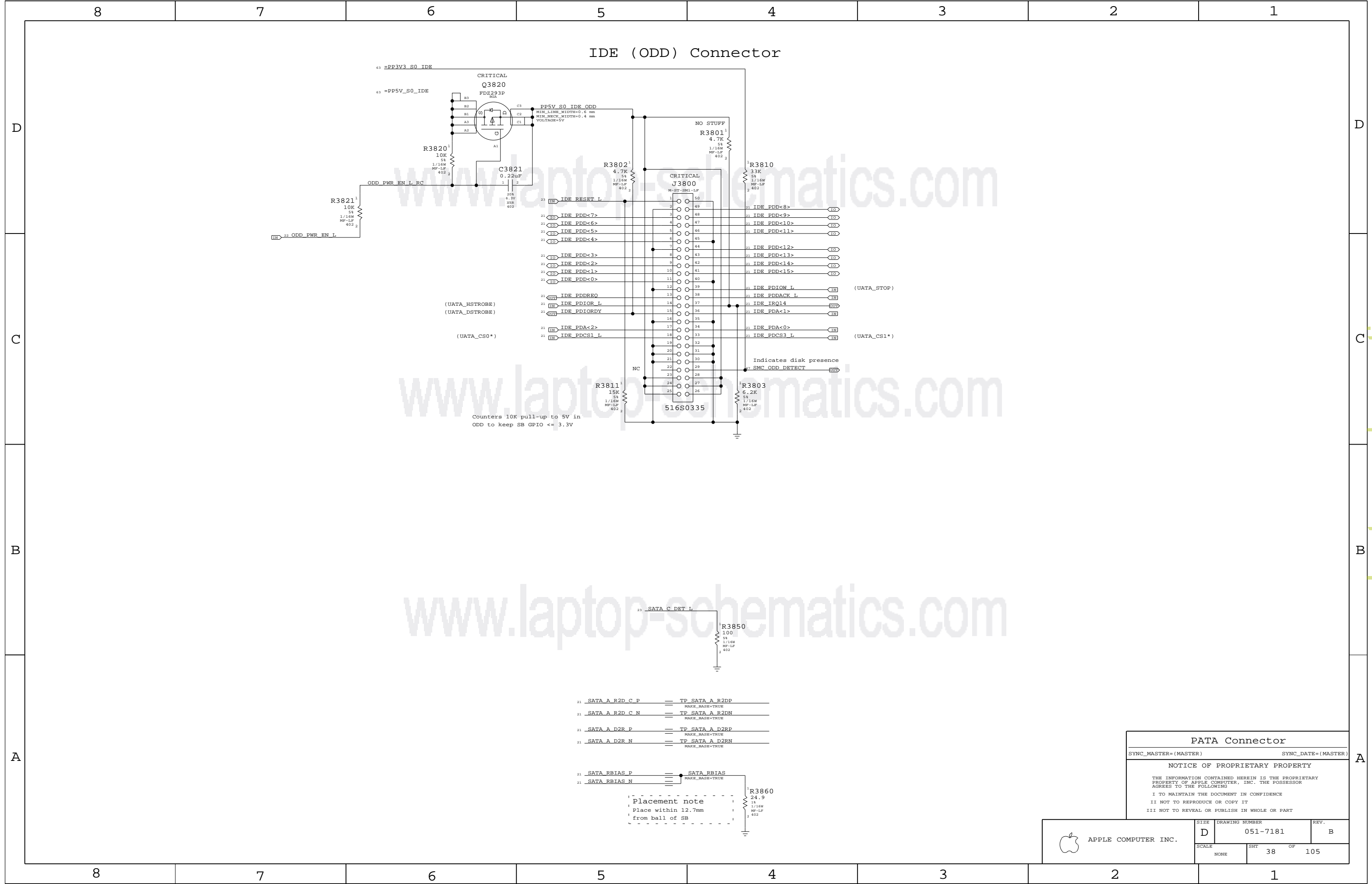
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	SCALE NONE	SHT 37	OF 105



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PATA Connector

SYNC\_MASTER=(MASTER) SYNC\_DATE=(MASTER)

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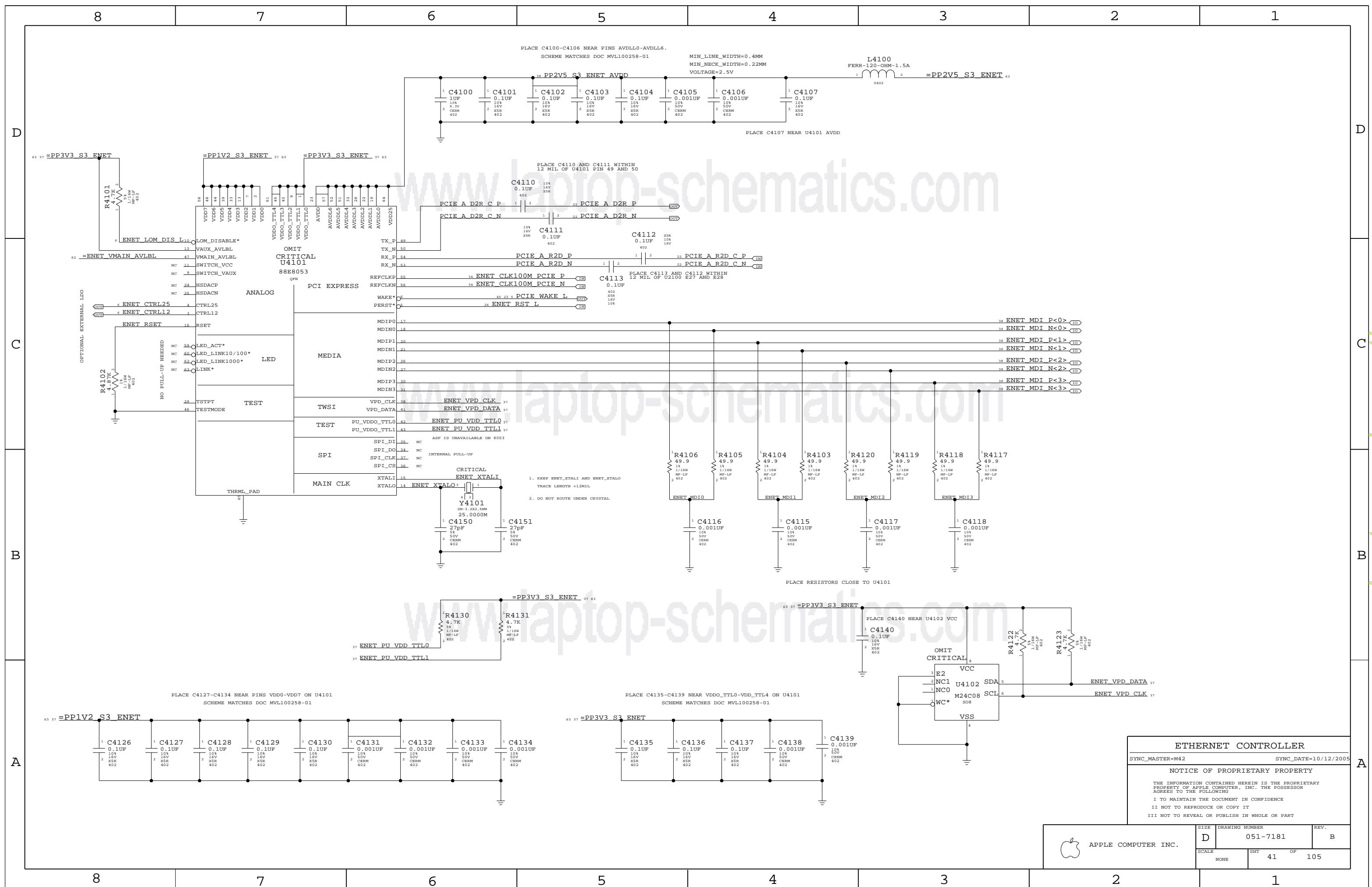
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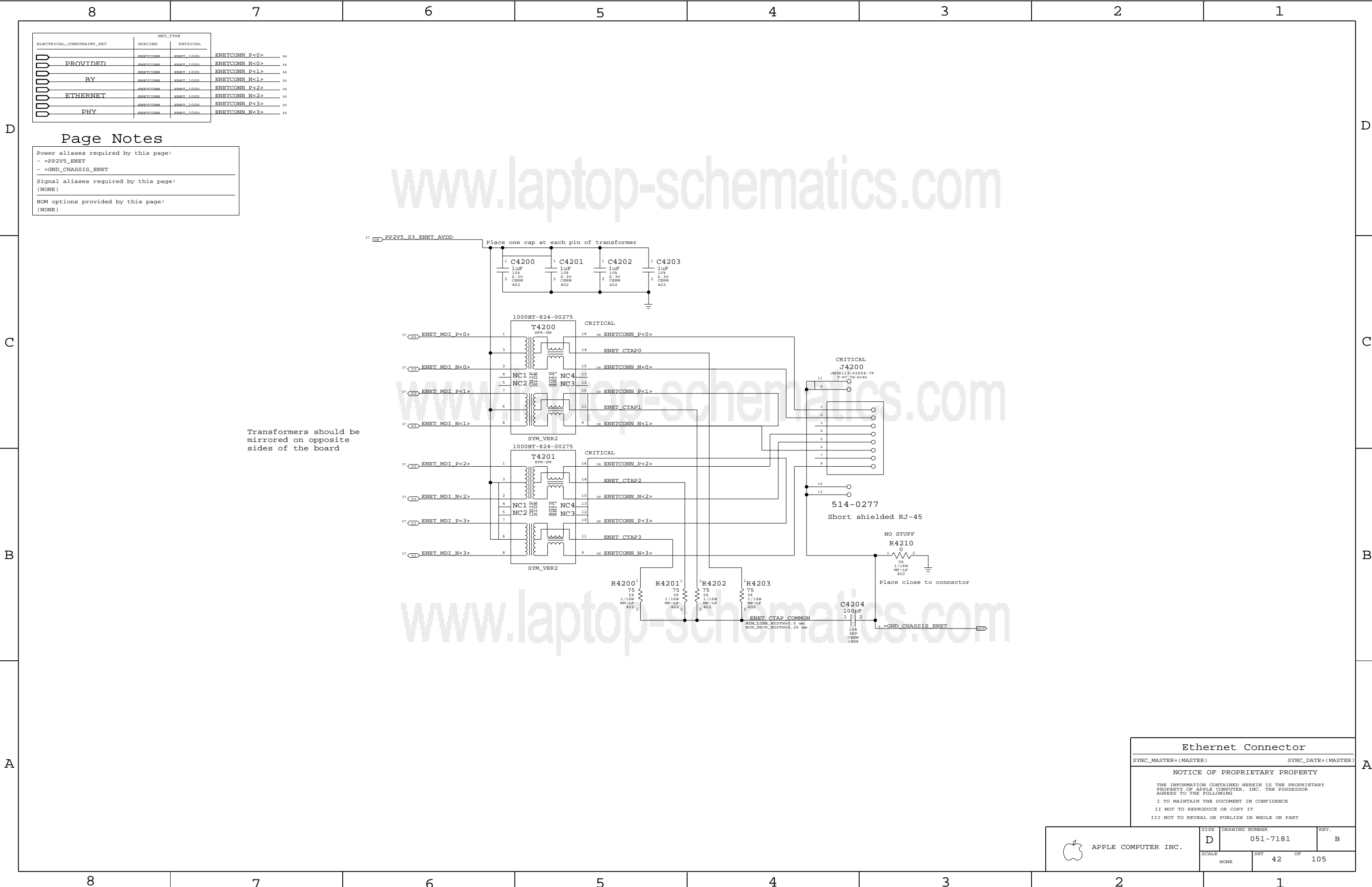
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	SCALE NONE	SHT 38 OF 105	





ELECTRICAL_CONSTRAINT_SET	NET_TYPE		
	SPACING	PHYSICAL	
PROVIDED	ENETCONN	ENET_100D	ENETCONN_P<0>
	ENETCONN	ENET_100D	ENETCONN_N<0>
	ENETCONN	ENET_100D	ENETCONN_P<1>
BY	ENETCONN	ENET_100D	ENETCONN_N<1>
	ENETCONN	ENET_100D	ENETCONN_P<2>
	ENETCONN	ENET_100D	ENETCONN_N<2>
ETHERNET	ENETCONN	ENET_100D	ENETCONN_P<3>
	ENETCONN	ENET_100D	ENETCONN_N<3>
	ENETCONN	ENET_100D	ENETCONN_N<3>
PHY	ENETCONN	ENET_100D	ENETCONN_N<3>
	ENETCONN	ENET_100D	ENETCONN_N<3>
	ENETCONN	ENET_100D	ENETCONN_N<3>

Page Notes

Power aliases required by this page:  
- =PP2V5\_ENET  
- =GND\_CHASSIS\_ENET

Signal aliases required by this page:  
(NONE)

BOM options provided by this page:  
(NONE)

Transformers should be mirrored on opposite sides of the board

Ethernet Connector

SYNC\_MASTER=(MASTER)

SYNC\_DATE=(MASTER)

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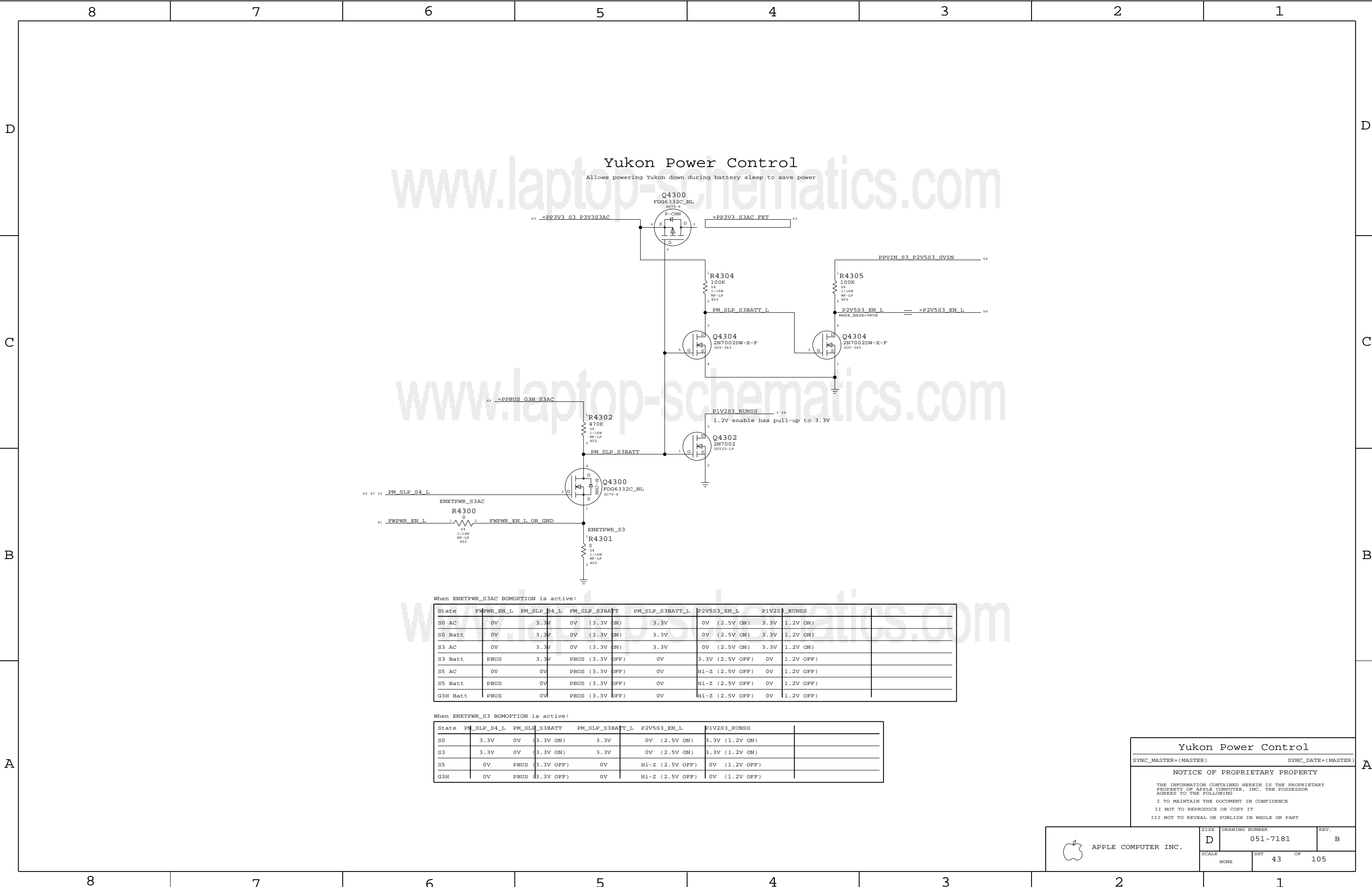
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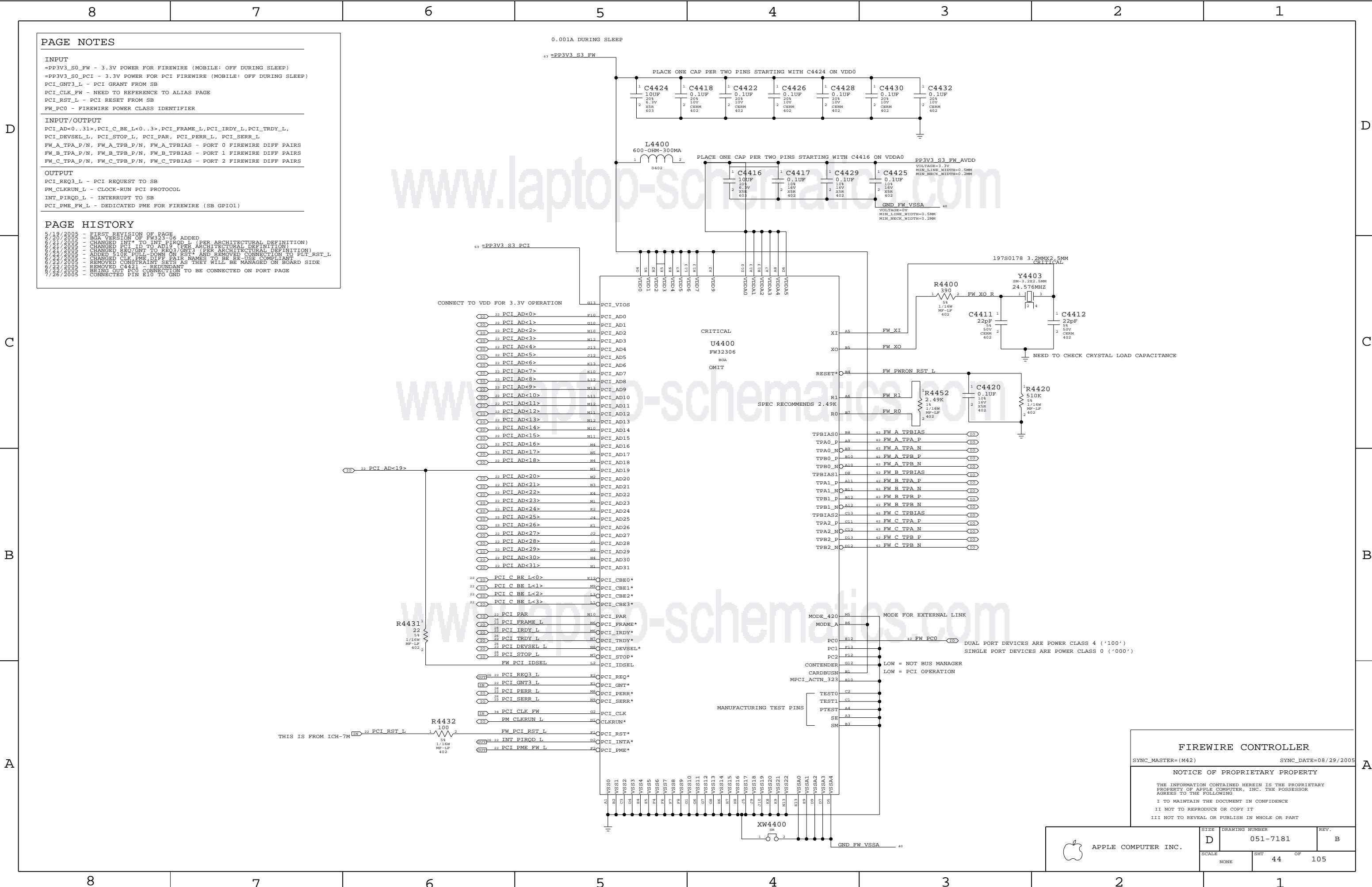
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	D	051-7181	B
SCALE		SHT	OF
NONE		42	105





PAGE NOTES

INPUT  
=PP3V3\_S0\_FW - 3.3V POWER FOR FIREWIRE (MOBILE: OFF DURING SLEEP)  
=PP3V3\_S0\_PCI - 3.3V POWER FOR PCI FIREWIRE (MOBILE: OFF DURING SLEEP)  
PCI\_GNT3\_L - PCI GRANT FROM SB  
PCI\_CLK\_FW - NEED TO REFERENCE TO ALIAS PAGE  
PCI\_RST\_L - PCI RESET FROM SB  
FW\_PC0 - FIREWIRE POWER CLASS IDENTIFIER

INPUT/OUTPUT  
PCI\_AD<0..31>, PCI\_C\_BE\_L<0..3>, PCI\_FRAME\_L, PCI\_IRDY\_L, PCI\_TRDY\_L,  
PCI\_DEVSEL\_L, PCI\_STOP\_L, PCI\_PAR, PCI\_PERR\_L, PCI\_SERR\_L  
FW\_A\_TPA\_P/N, FW\_A\_TPB\_P/N, FW\_A\_TPBAS - PORT 0 FIREWIRE DIFF PAIRS  
FW\_B\_TPA\_P/N, FW\_B\_TPB\_P/N, FW\_B\_TPBAS - PORT 1 FIREWIRE DIFF PAIRS  
FW\_C\_TPA\_P/N, FW\_C\_TPB\_P/N, FW\_C\_TPBAS - PORT 2 FIREWIRE DIFF PAIRS

OUTPUT  
PCI\_REQ3\_L - PCI REQUEST TO SB  
PM\_CLKRUN\_L - CLOCK-RUN PCI PROTOCOL  
INT\_PIRQD\_L - INTERRUPT TO SB  
PCI\_PME\_FW\_L - DEDICATED PME FOR FIREWIRE (SB GPIO1)

PAGE HISTORY

5/19/2005 - FIRST REVISION OF PAGE  
6/20/2005 - BGA VERSION OF FW323-06 ADDED  
6/21/2005 - CHANGED INT\* TO INT\_PIRQD (PER ARCHITECTURAL DEFINITION)  
6/21/2005 - CHANGED PCI\_ID TO AD19 (PER ARCHITECTURAL DEFINITION)  
6/21/2005 - CHANGED REQ/GNT TO REQ3/GNT3 (PER ARCHITECTURAL DEFINITION)  
6/22/2005 - ADDED 510K PULL-DOWN ON RST\* AND REMOVED CONNECTION TO PLT\_RST\_L  
6/22/2005 - CHANGED CLK\_PME DIFF PAIR NAMES TO BE RE-USE COMPLIANT  
6/22/2005 - REMOVED CONSTRAINT SETS AS THEY WILL BE MANAGED ON BOARD SIDE  
6/22/2005 - REMOVED C4421 - REDUNDANT  
6/22/2005 - BRING OUT PC0 CONNECTION TO BE CONNECTED ON PORT PAGE  
7/26/2005 - CONNECTED PIN E10 TO GND

FIREWIRE CONTROLLER

SYNC\_MASTER=(M42) SYNC\_DATE=08/29/2005

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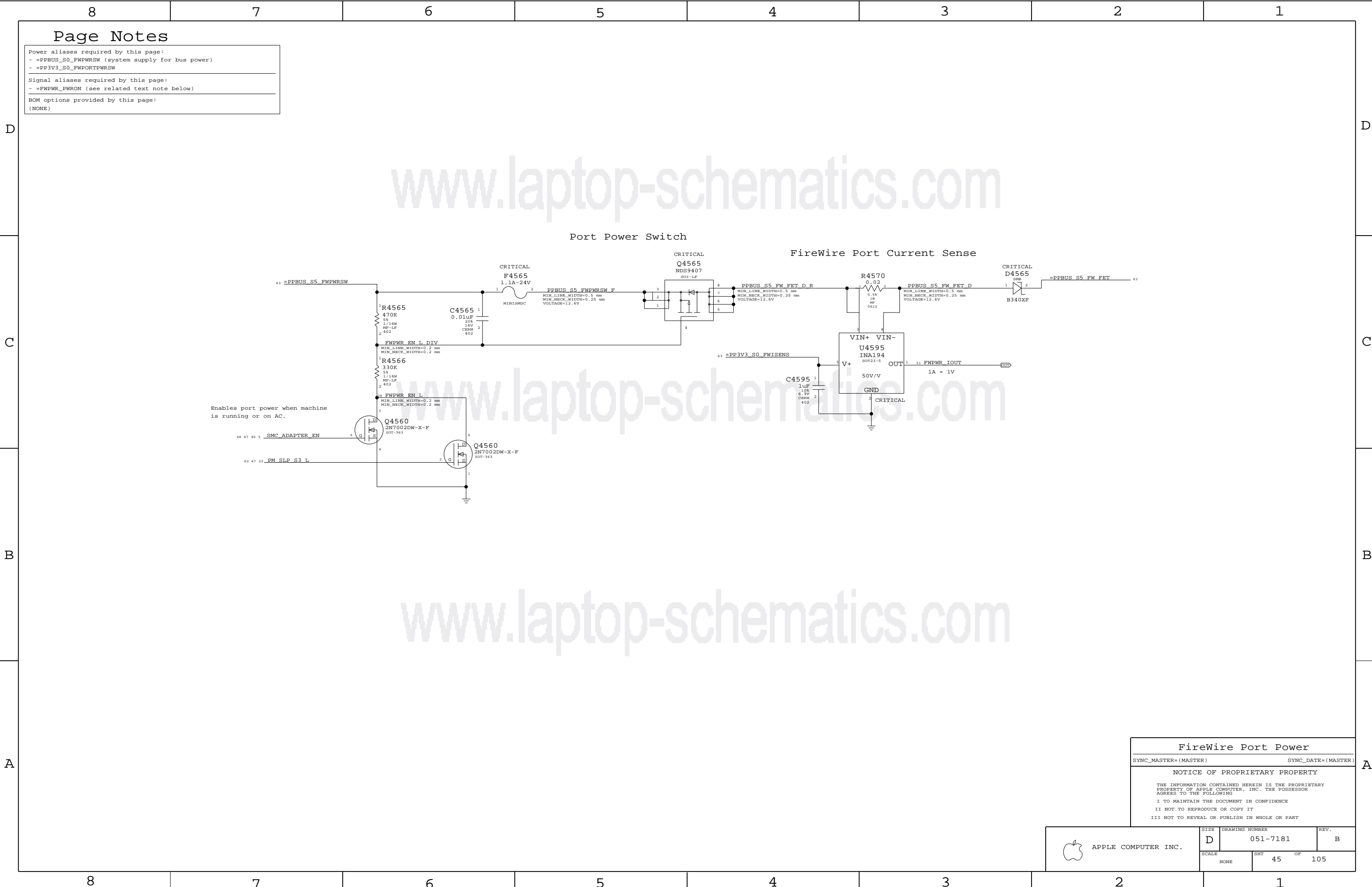
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D	051-7181	B
SCALE	SHT	OF
NONE	44	105





Page Notes

Power aliases required by this page:

- =PPBUS\_S0\_FWPWSW (system supply for bus power)
- =PP3V3\_S0\_FWPORTPWSW

Signal aliases required by this page:

- =FWPWR\_PWRON (see related text note below)

BOM options provided by this page:

(NONE)

FireWire Port Power

SYNC\_MASTER=(MASTER)

SYNC\_DATE=(MASTER)

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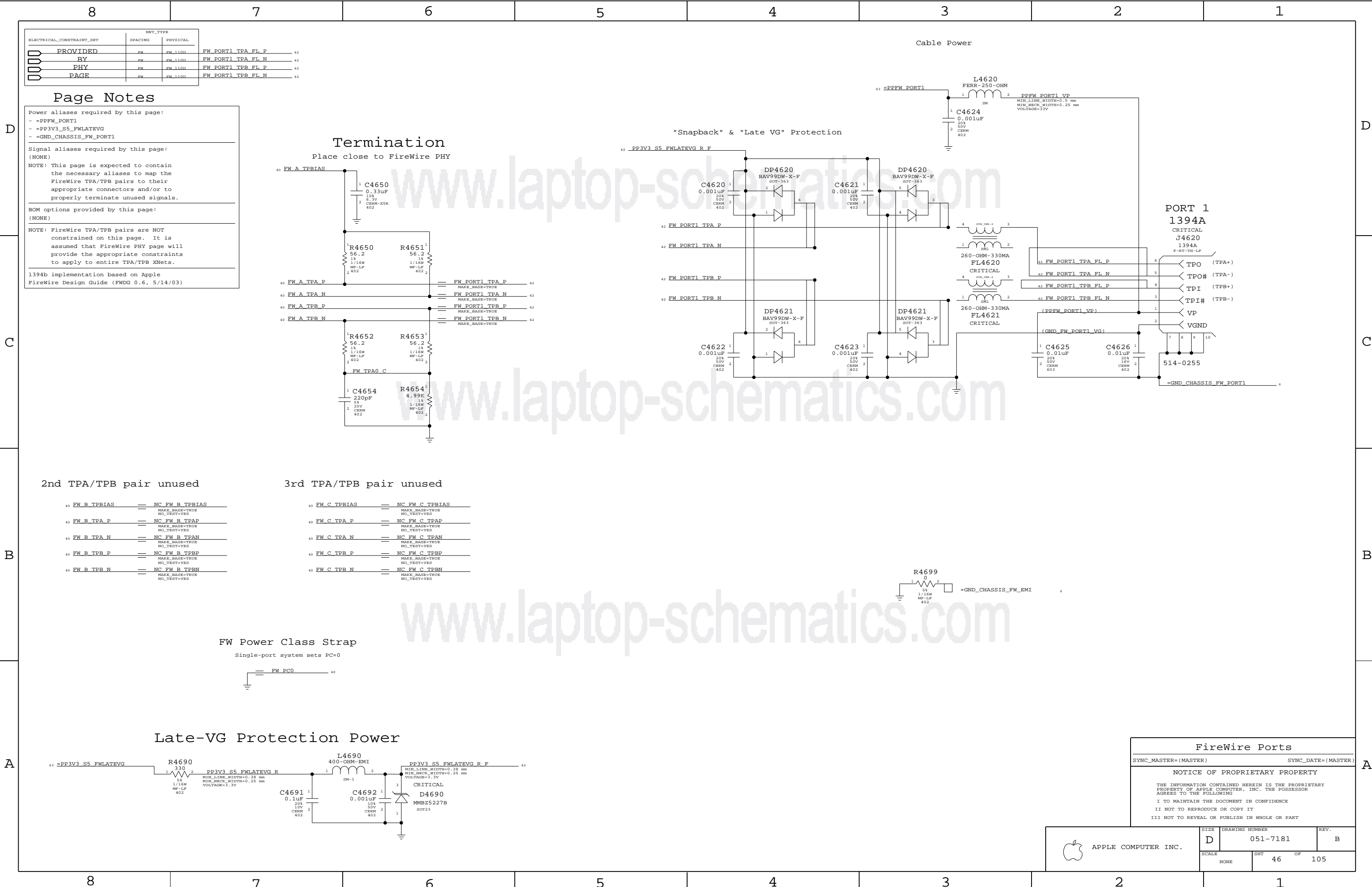
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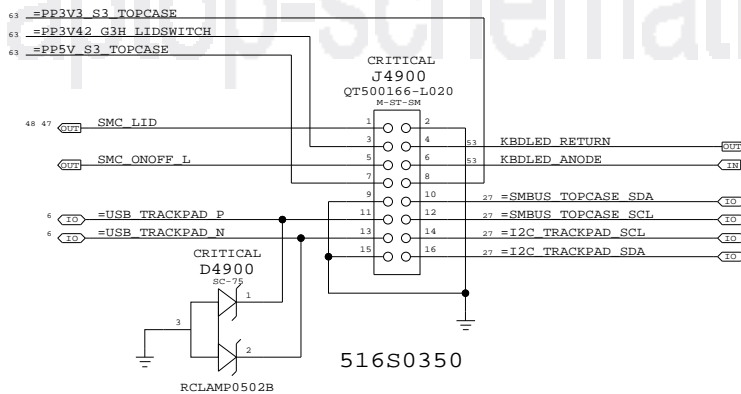


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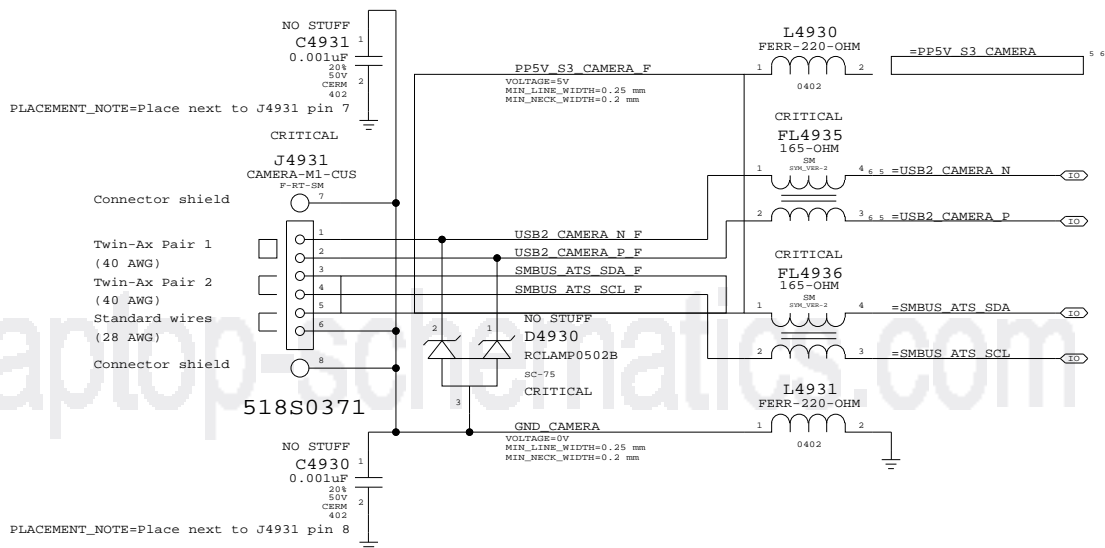
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## Top-Case Connector



## Camera Connector



### Internal USB Connections

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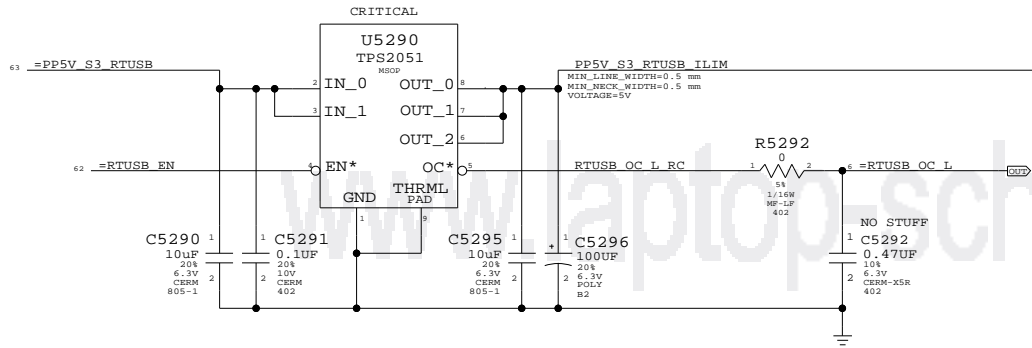


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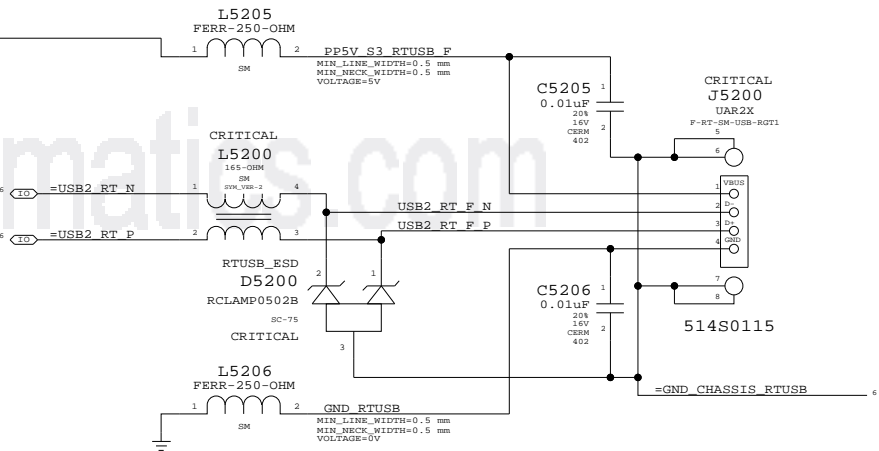
SIZE D DRAWING NUMBER 051-7181 REV. B

SCALE NONE SHT 49 OF 105

Port Power Switch



Right USB Port



Place L5200, L5205 and L5206 across moat

External USB Connector

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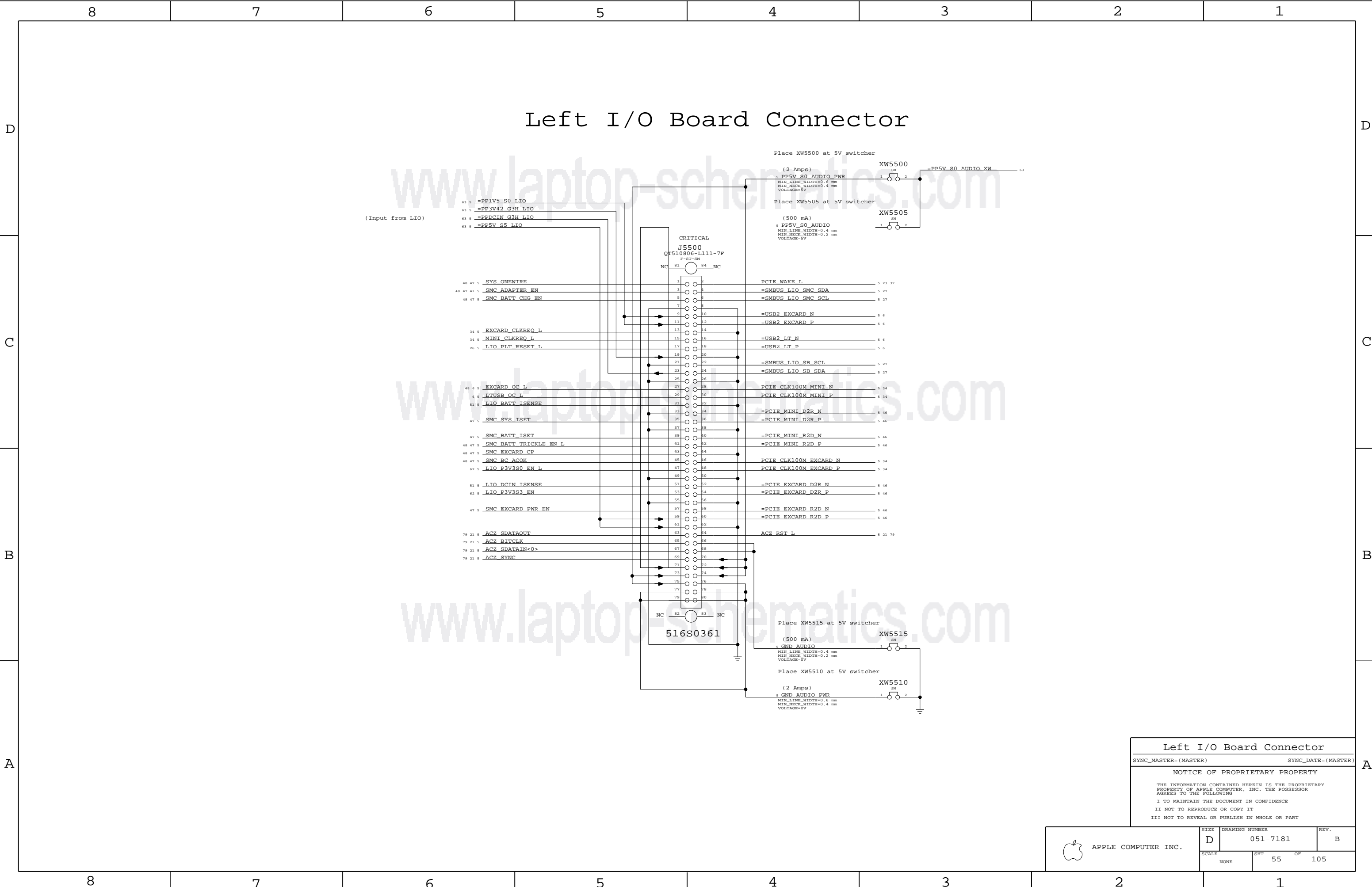
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SIZE D DRAWING NUMBER 051-7181 REV. B

SCALE NONE SHT 52 OF 105



Left I/O Board Connector

Left I/O Board Connector

SYNC\_MASTER=(MASTER)

SYNC\_DATE=(MASTER)

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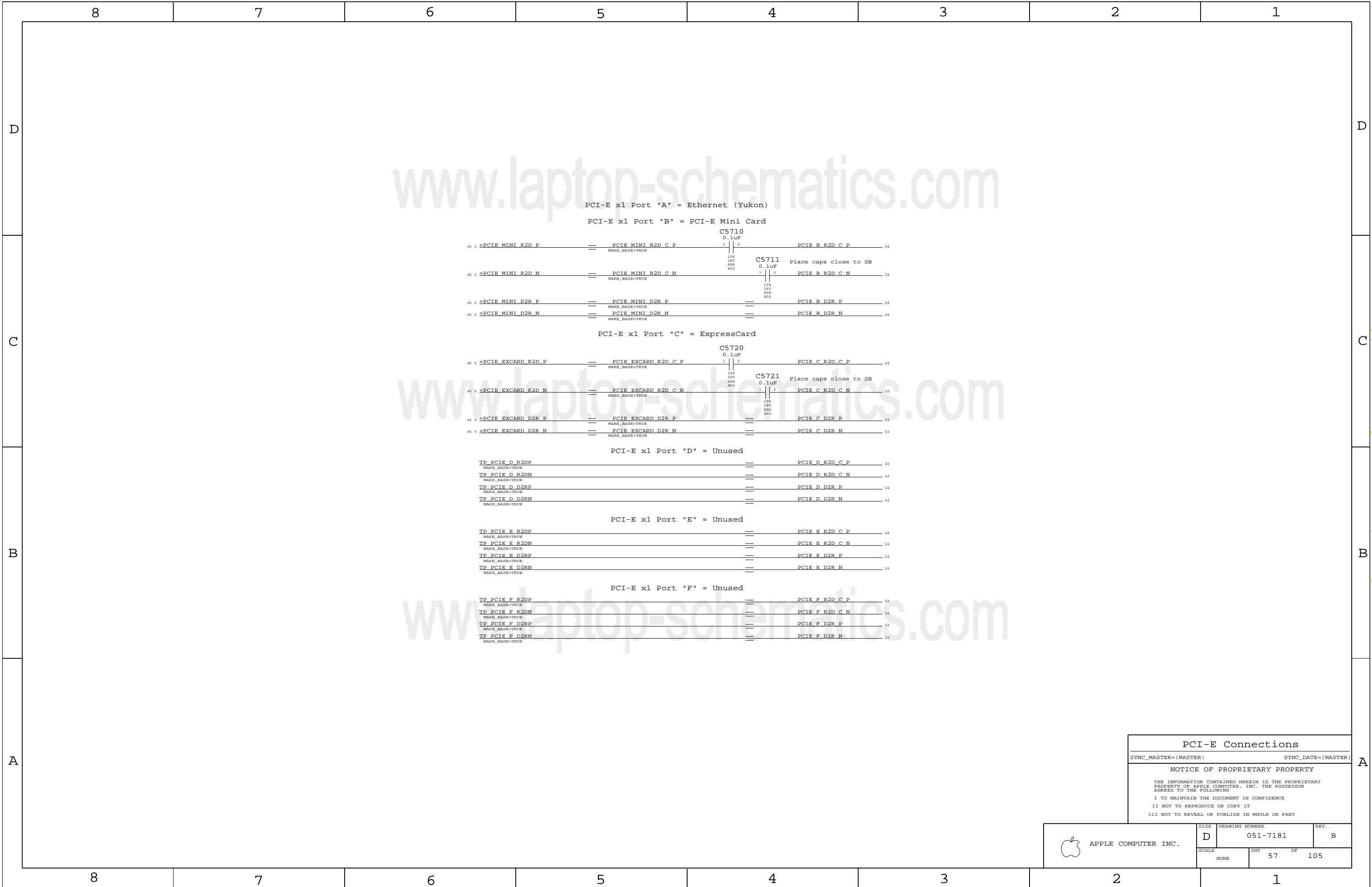
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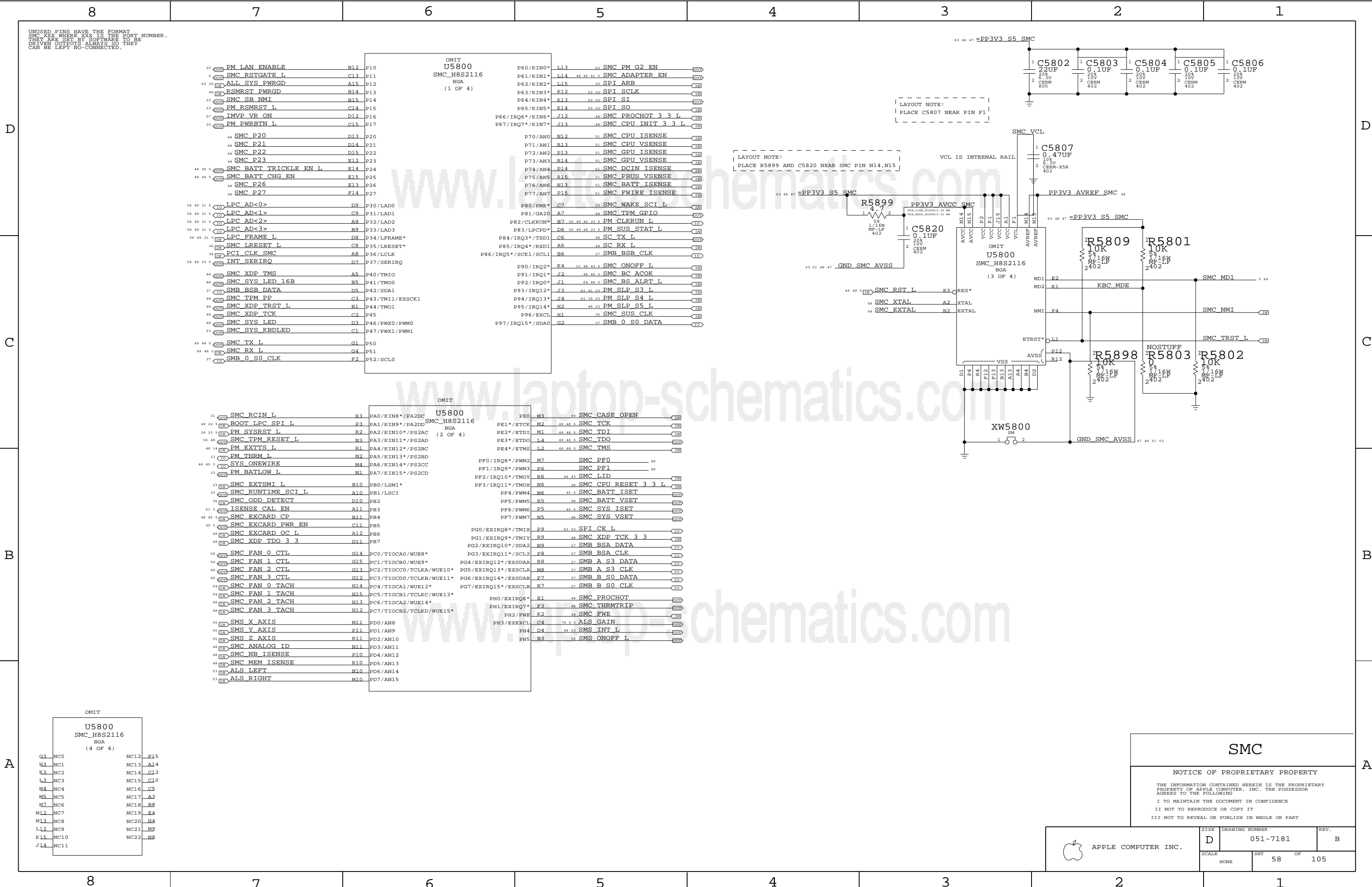
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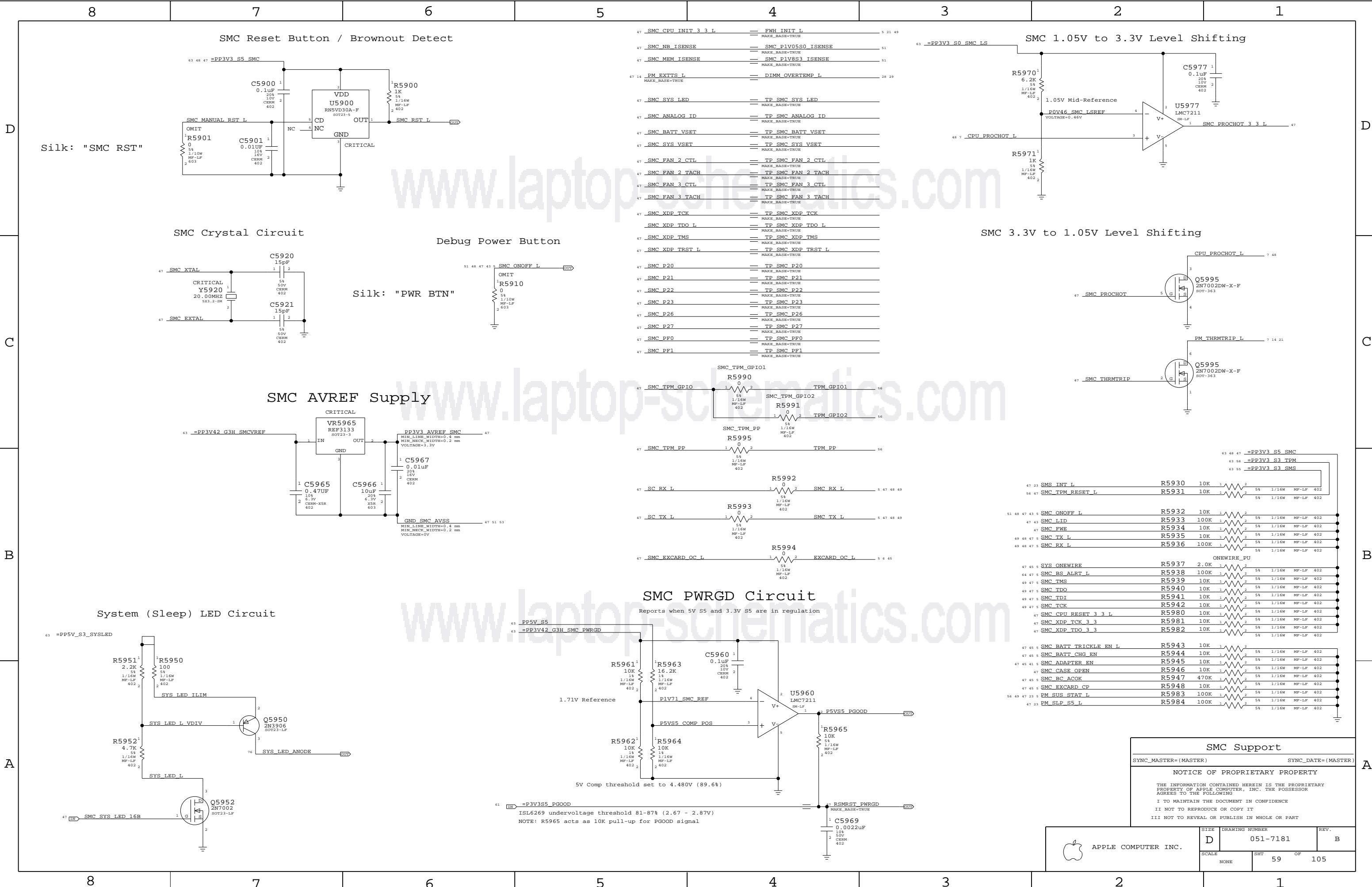
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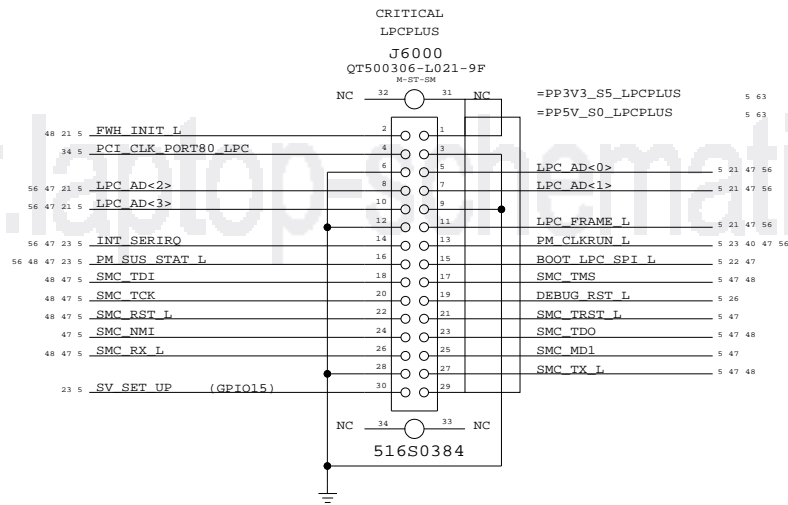
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# LPC+ Debug Connector

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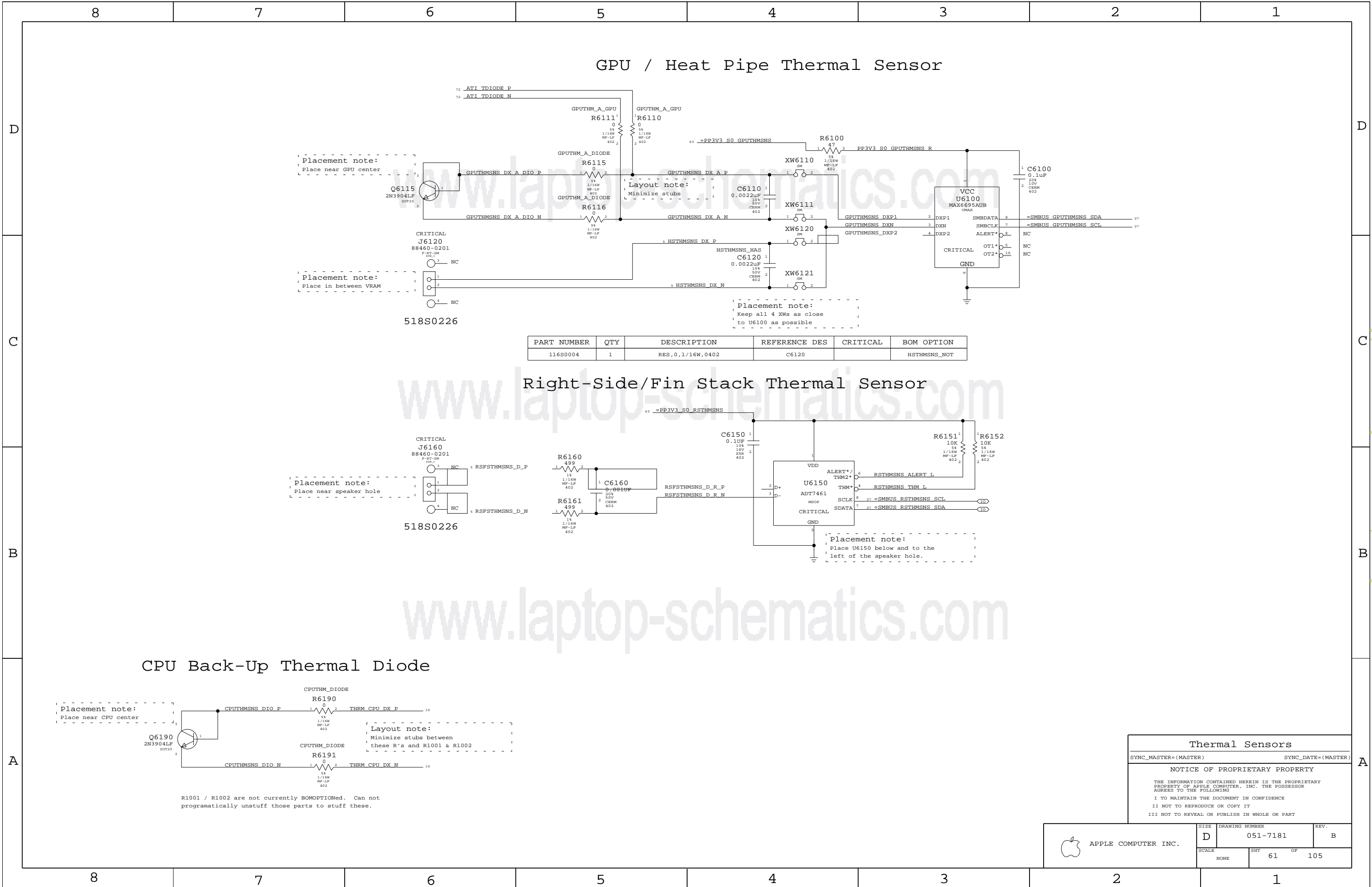
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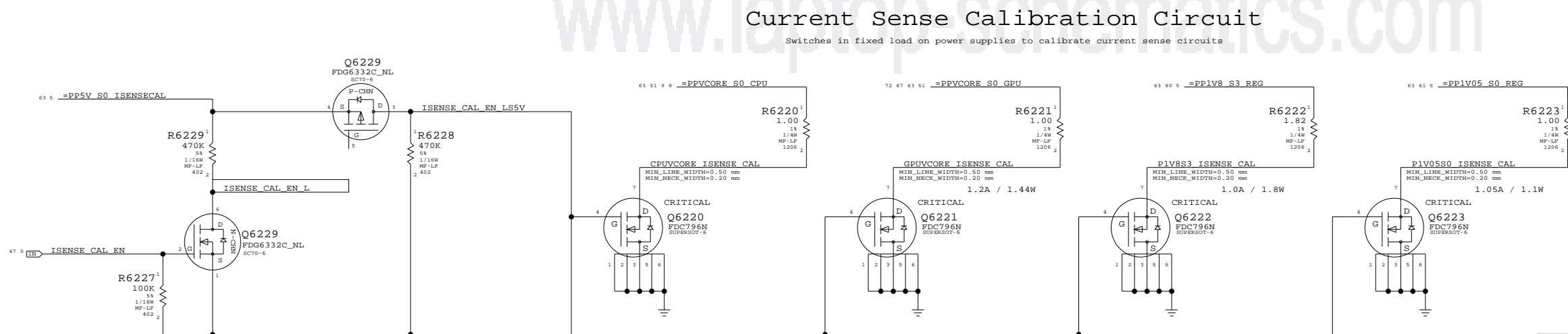
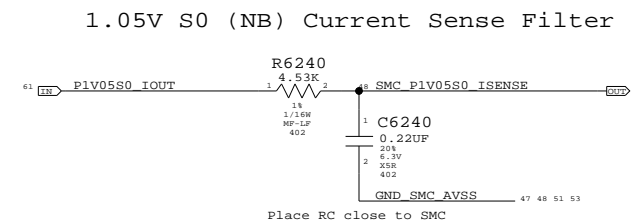
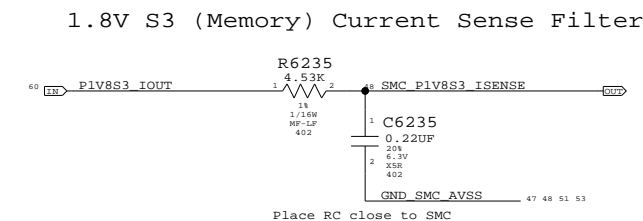
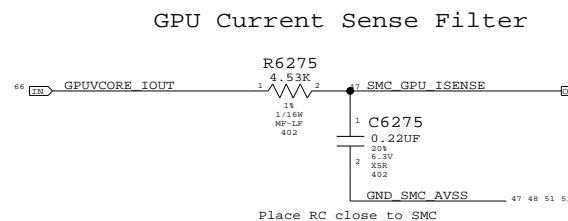
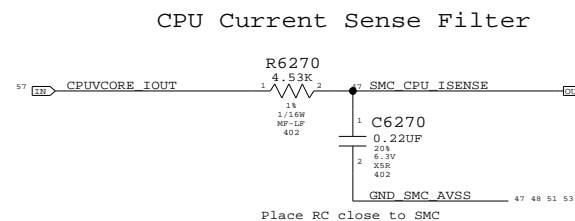
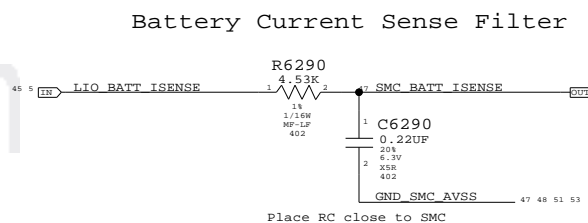
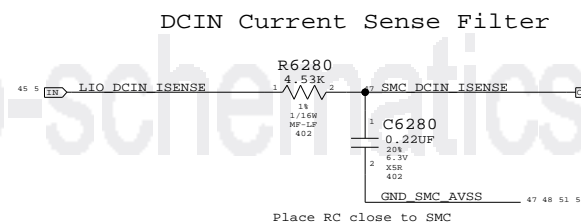
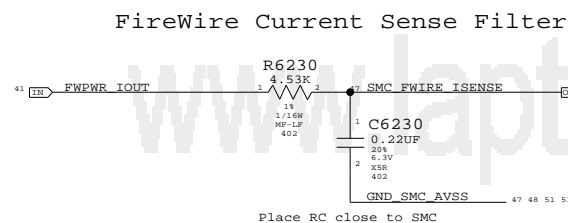
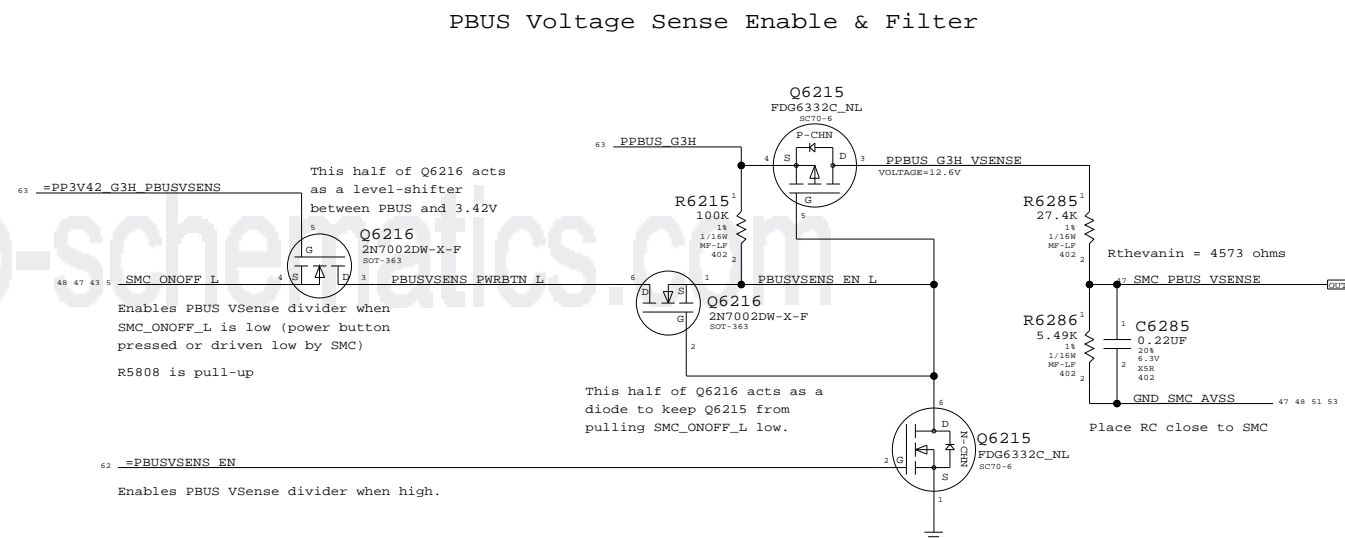
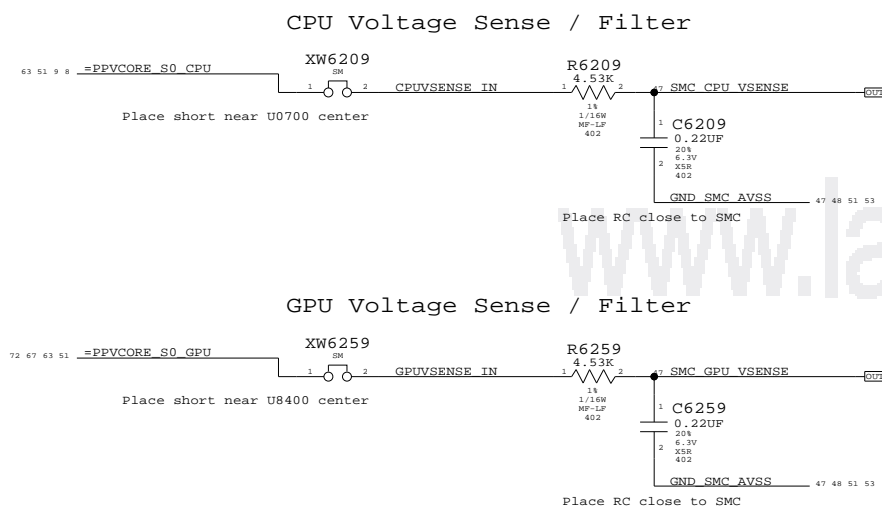
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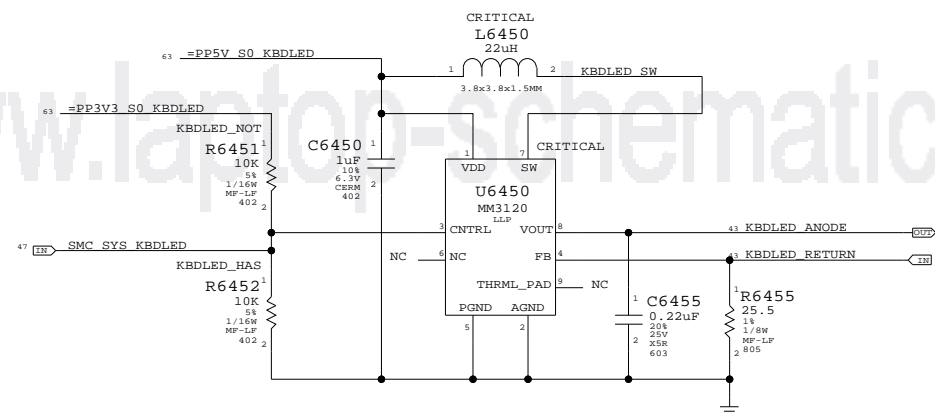
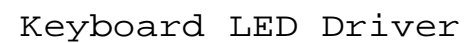
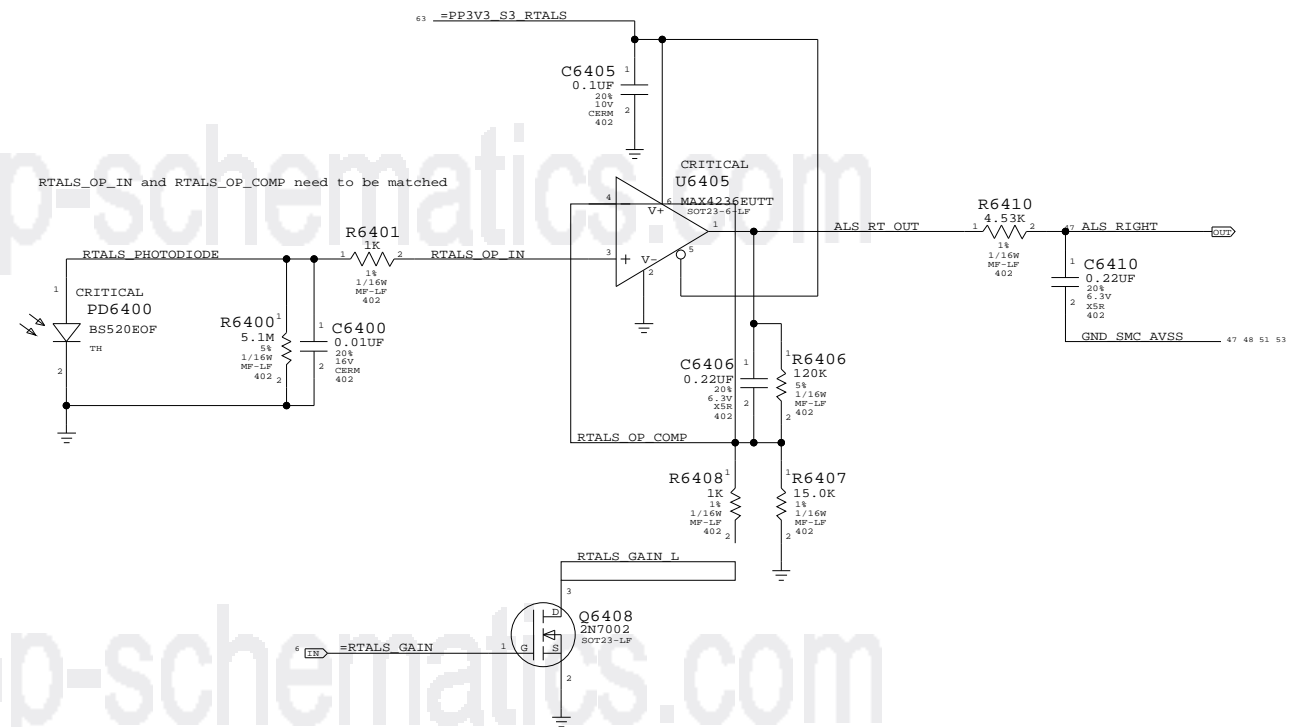
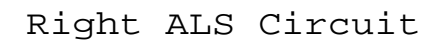
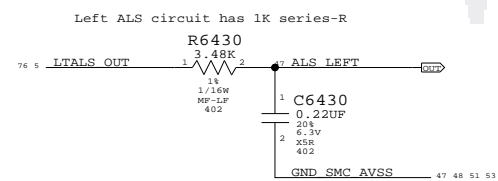





Current & Voltage Sensing	
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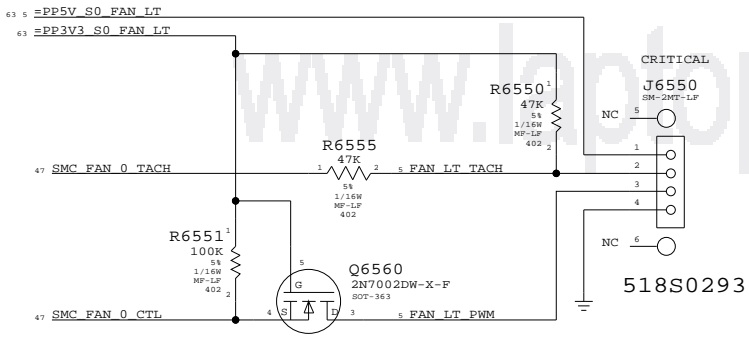


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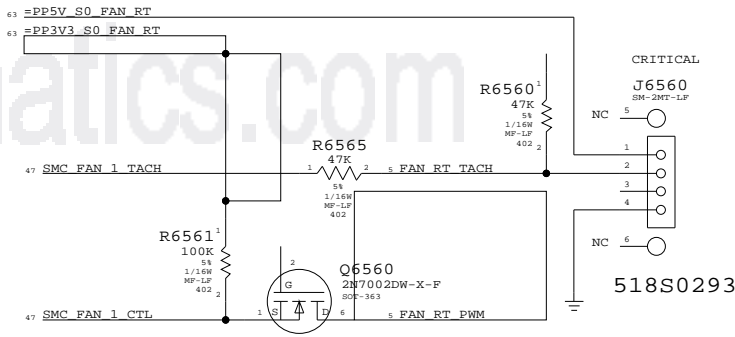
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Left Fan



Right Fan



Fan Connectors

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SIZE

D

DRAWING NUMBER

051-7181

REV.

B

SCALE

NONE

SHT

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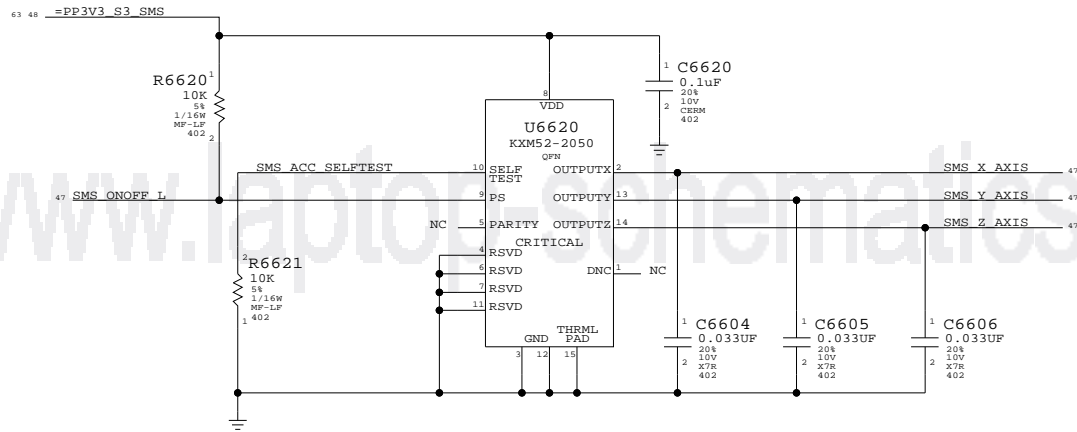
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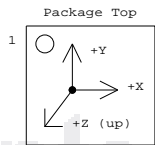
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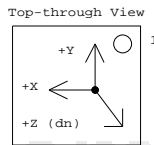
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Desired orientation when placed on board top-side:



Desired orientation when placed on board bottom-side:



M1 placement: Bottom-side

### Sudden Motion Sensor (SMS)

SYNC\_MASTER=(MASTER) SYNC\_DATE=(MASTER)

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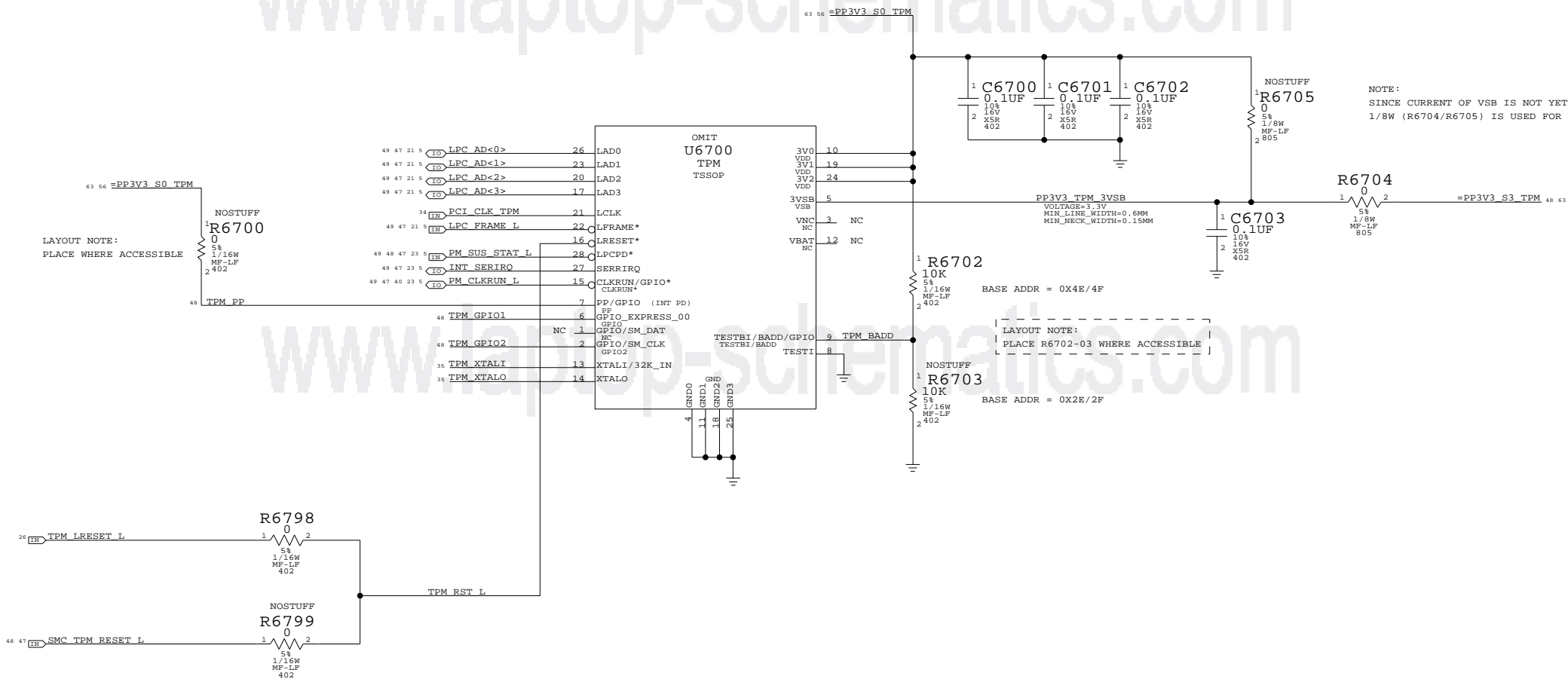
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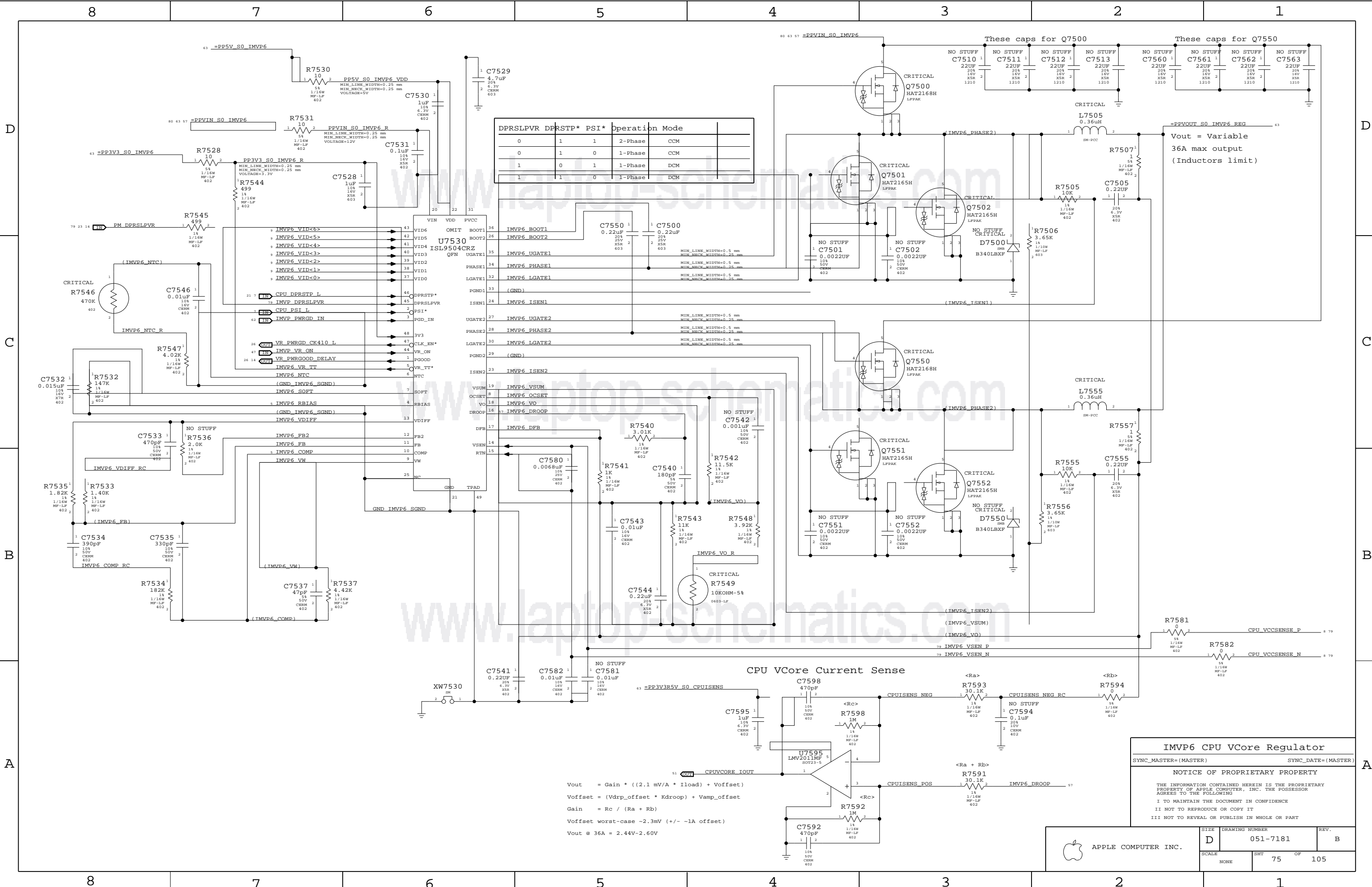
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NONE	66	105

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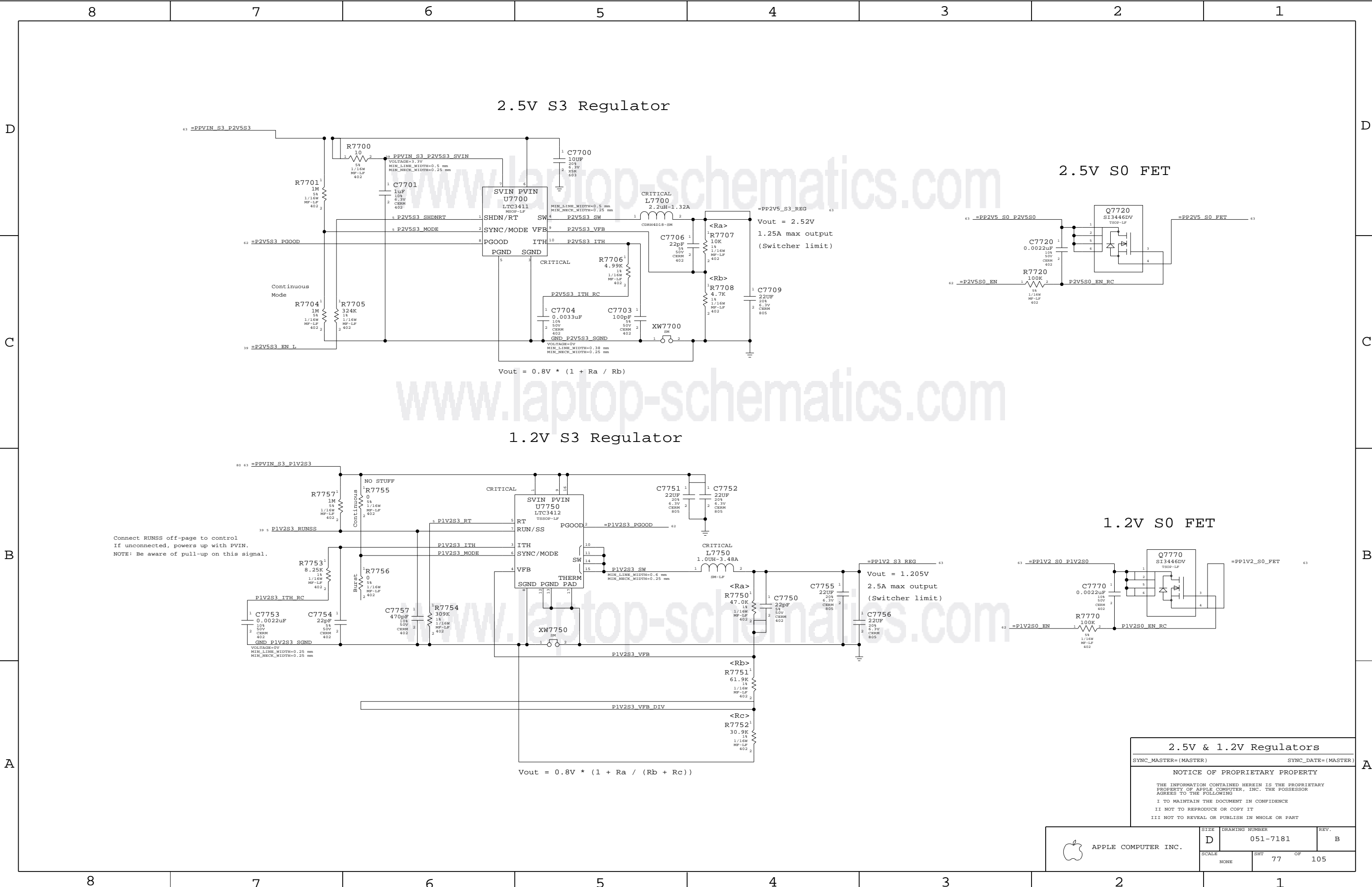
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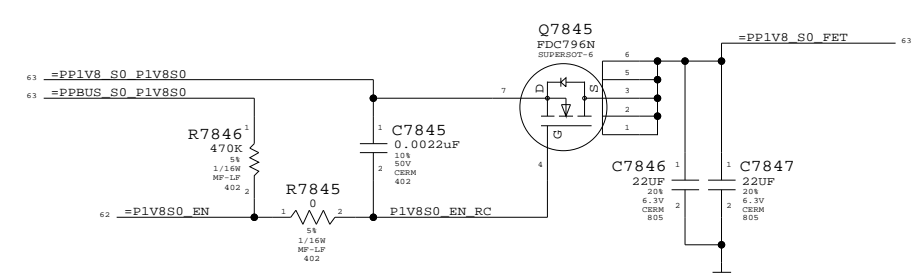
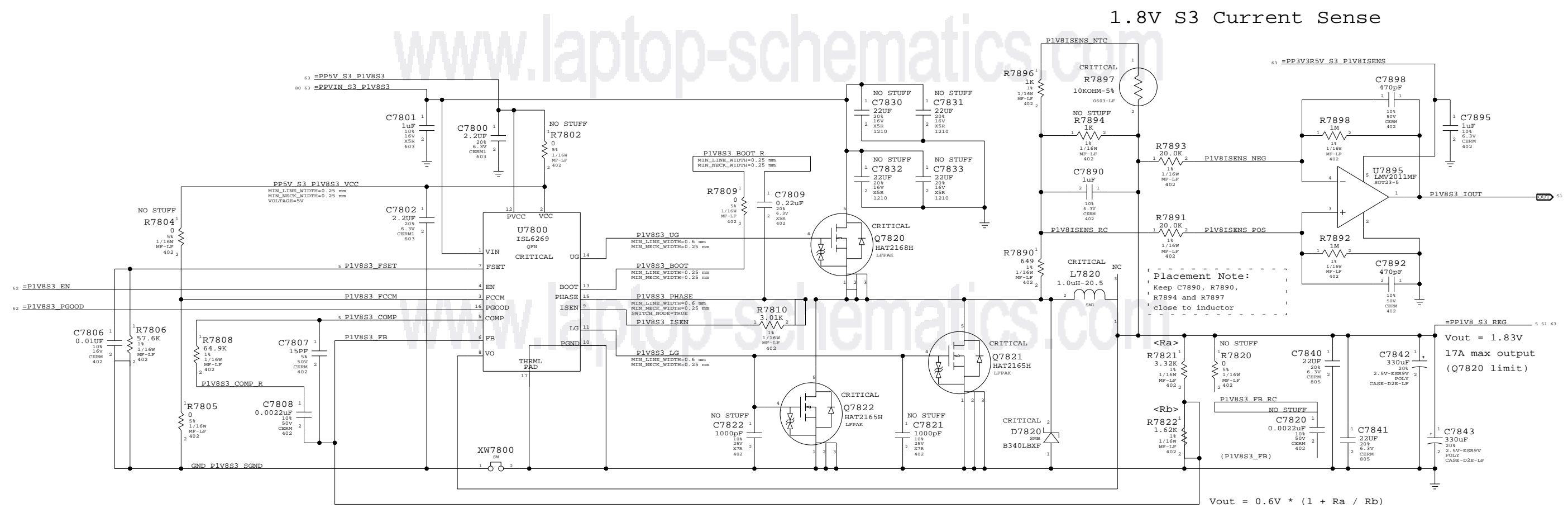
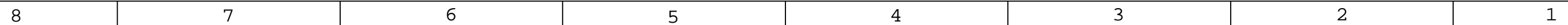
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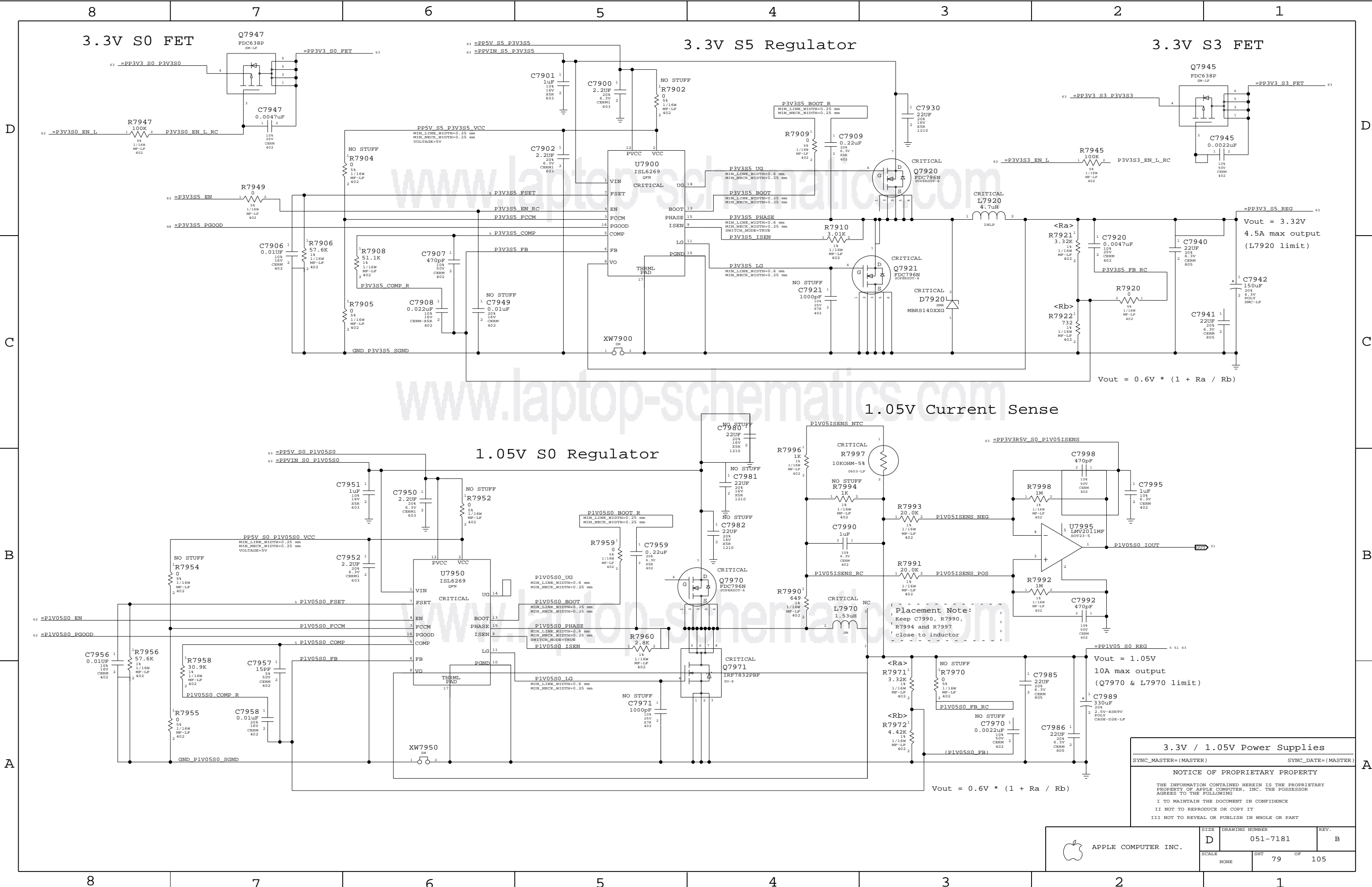






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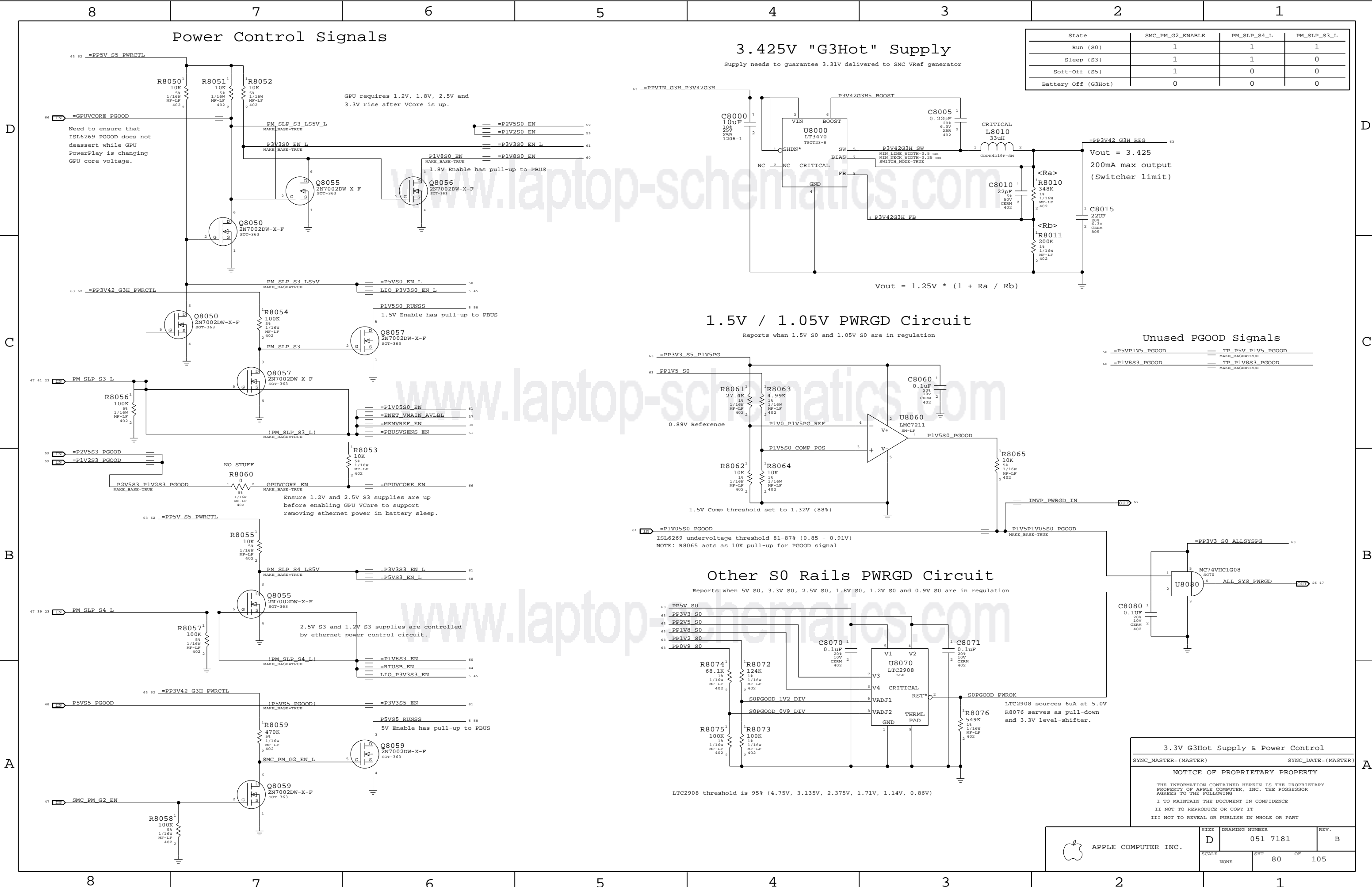
 APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-7181	REV. B
	SCALE NONE	SHT 78 OF 105	



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3.3V / 1.05V Power Supplies  
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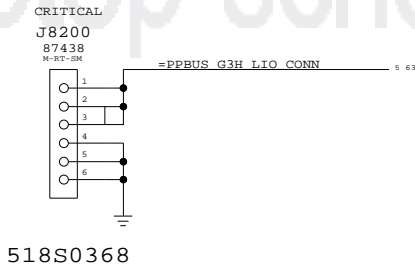
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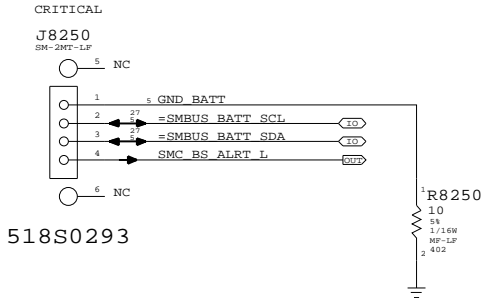
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Left I/O Power Connector



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Battery Connector (Digital Signals)



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PBus-In & Battery Connectors

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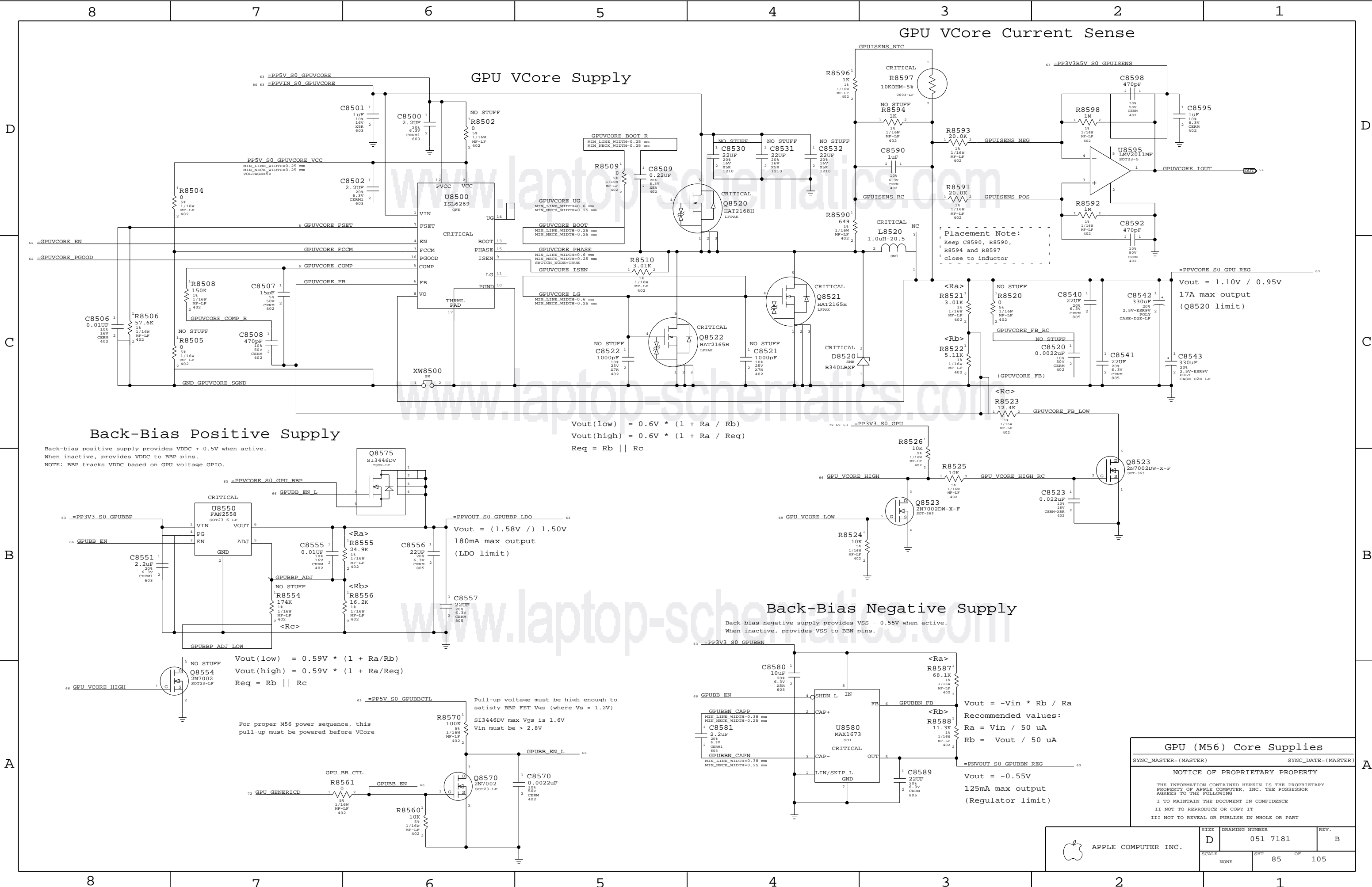


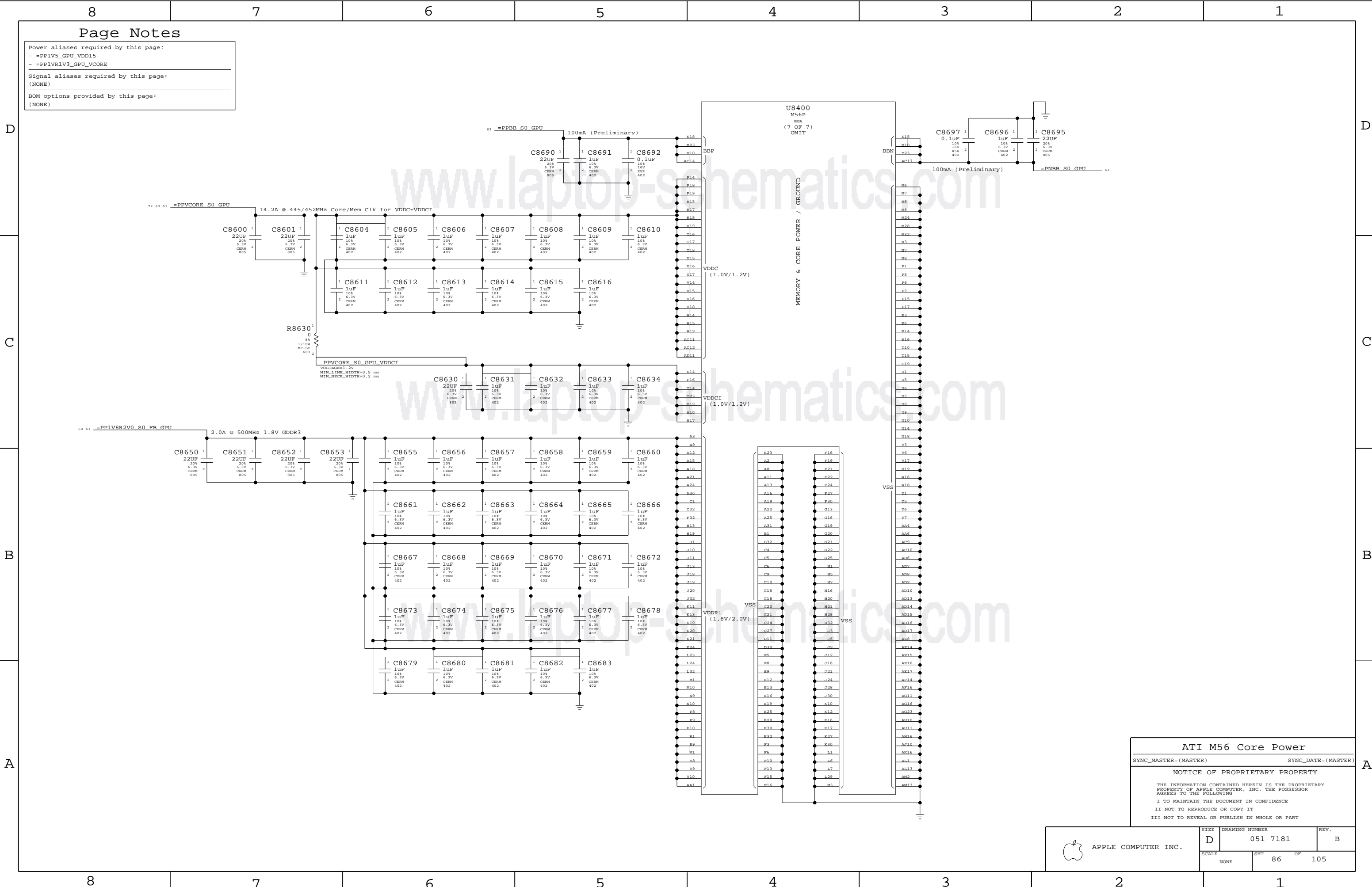
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D	051-7181	B
SCALE	SHT	OF
NONE	82	105









Page Notes

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- =PP1V5\_GPU\_VDD15
- =PP1VR1V3\_GPU\_VCORE

Signal aliases required by this page:

(NONE)

BOM options provided by this page:

(NONE)

ATI M56 Core Power

SYNC\_MASTER=(MASTER)

SYNC\_DATE=(MASTER)

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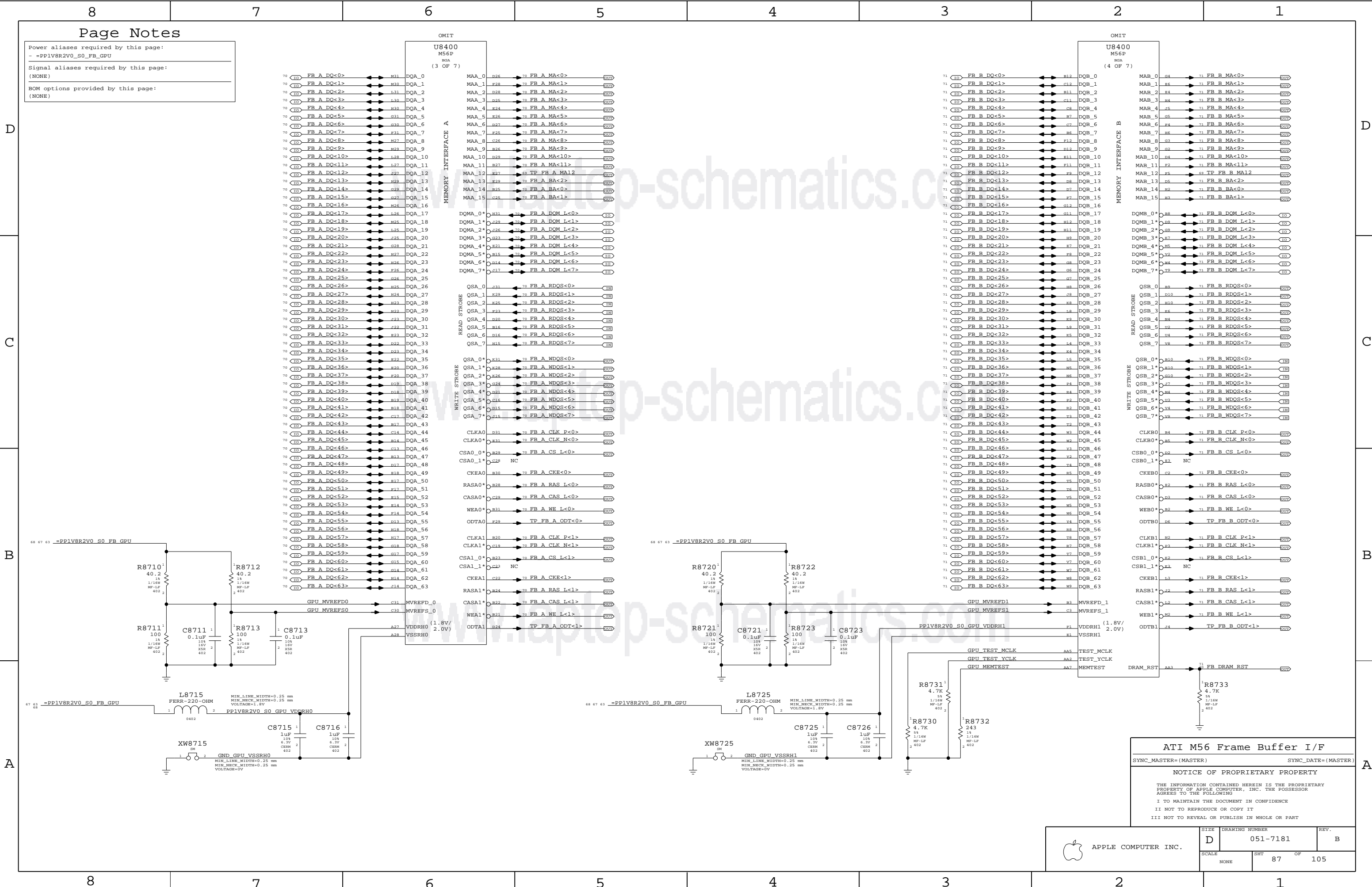
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	D	051-7181	B
	SCALE	SHT	OF
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Page Notes

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- =PPIV8R2V0\_S0\_FB\_GPU

Signal aliases required by this page:  
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BOM options provided by this page:  
(NONE)

U8400 M56P (3 OF 7)		
MEMORY INTERFACE A		
MAA_0	D26	70 FB A MA<0>
MAA_1	E28	70 FB A MA<1>
MAA_2	D28	70 FB A MA<2>
MAA_3	D25	70 FB A MA<3>
MAA_4	E24	70 FB A MA<4>
MAA_5	E26	70 FB A MA<5>
MAA_6	D27	70 FB A MA<6>
MAA_7	E25	70 FB A MA<7>
MAA_8	C26	70 FB A MA<8>
MAA_9	B26	70 FB A MA<9>
MAA_10	D23	70 FB A MA<10>
MAA_11	B27	70 FB A MA<11>
MAA_12	E27	69 TP FB A MA12
MAA_13	E25	70 FB A BA<2>
MAA_14	B25	70 FB A BA<0>
MAA_15	C25	70 FB A BA<1>
MEMORY INTERFACE B		
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MAB_3	H4	71 FB B MA<3>
MAB_4	J5	71 FB B MA<4>
MAB_5	G5	71 FB B MA<5>
MAB_6	F4	71 FB B MA<6>
MAB_7	H6	71 FB B MA<7>
MAB_8	G3	71 FB B MA<8>
MAB_9	G2	71 FB B MA<9>
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ATI M56 Frame Buffer I/F

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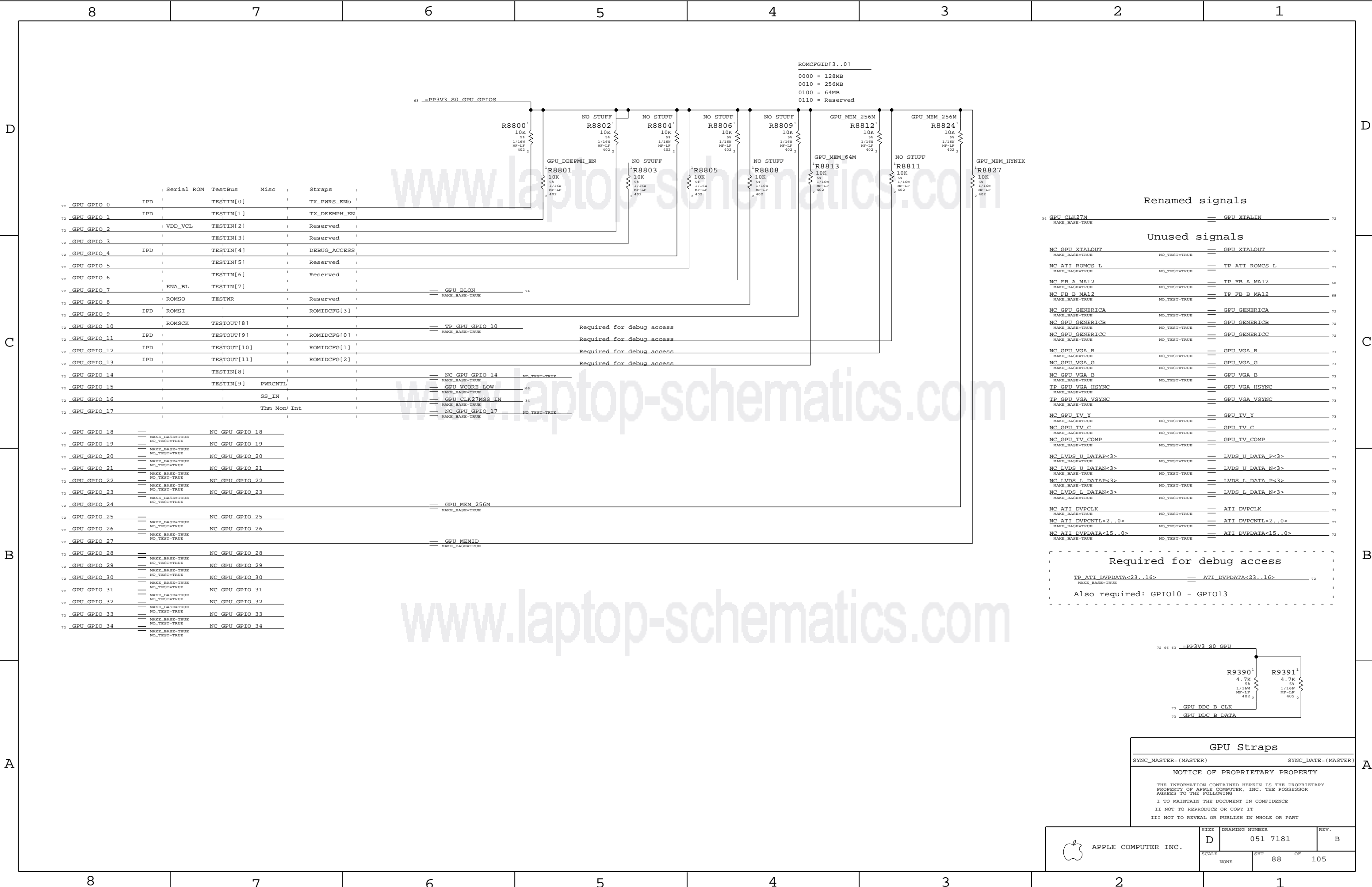
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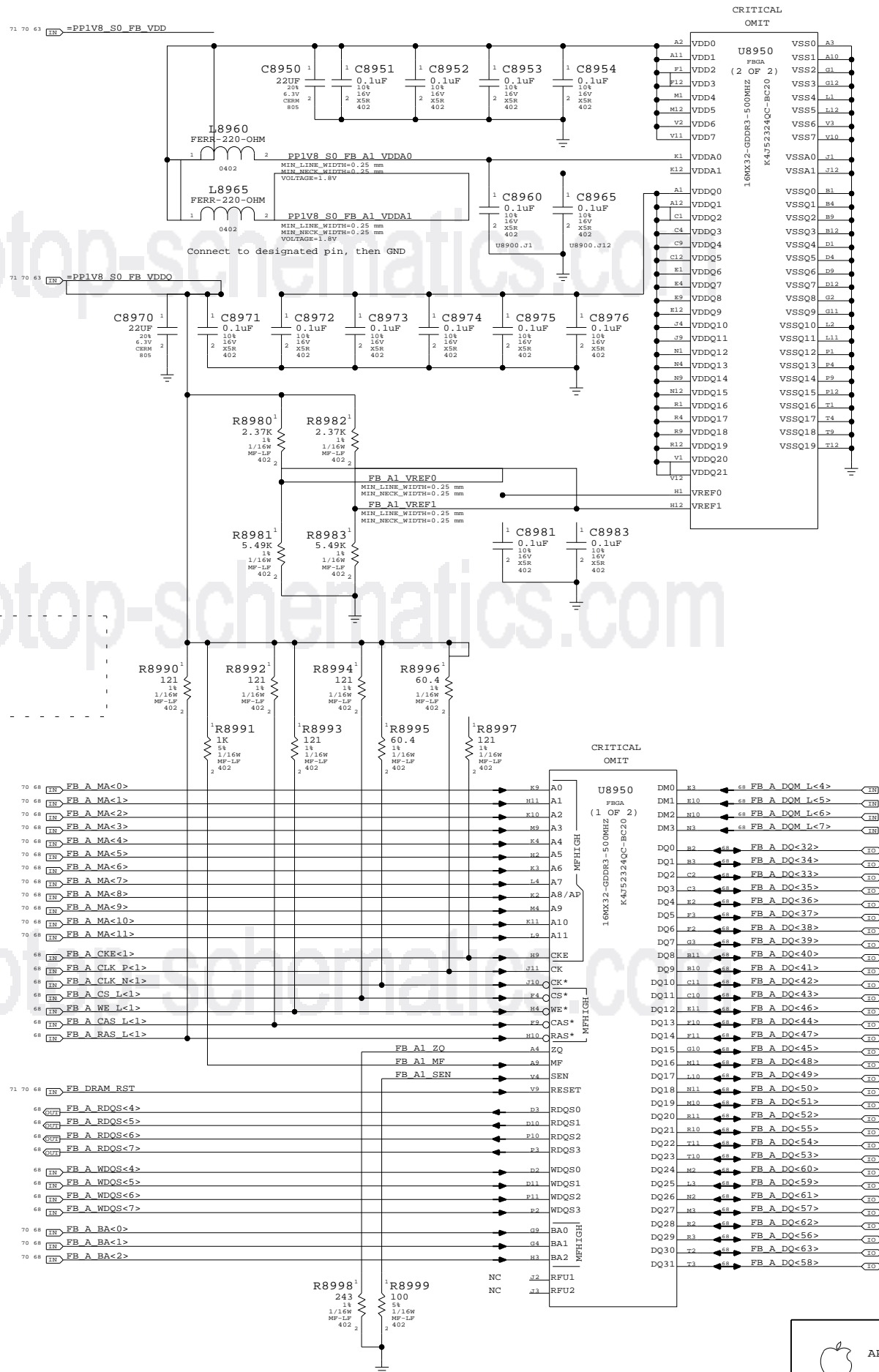
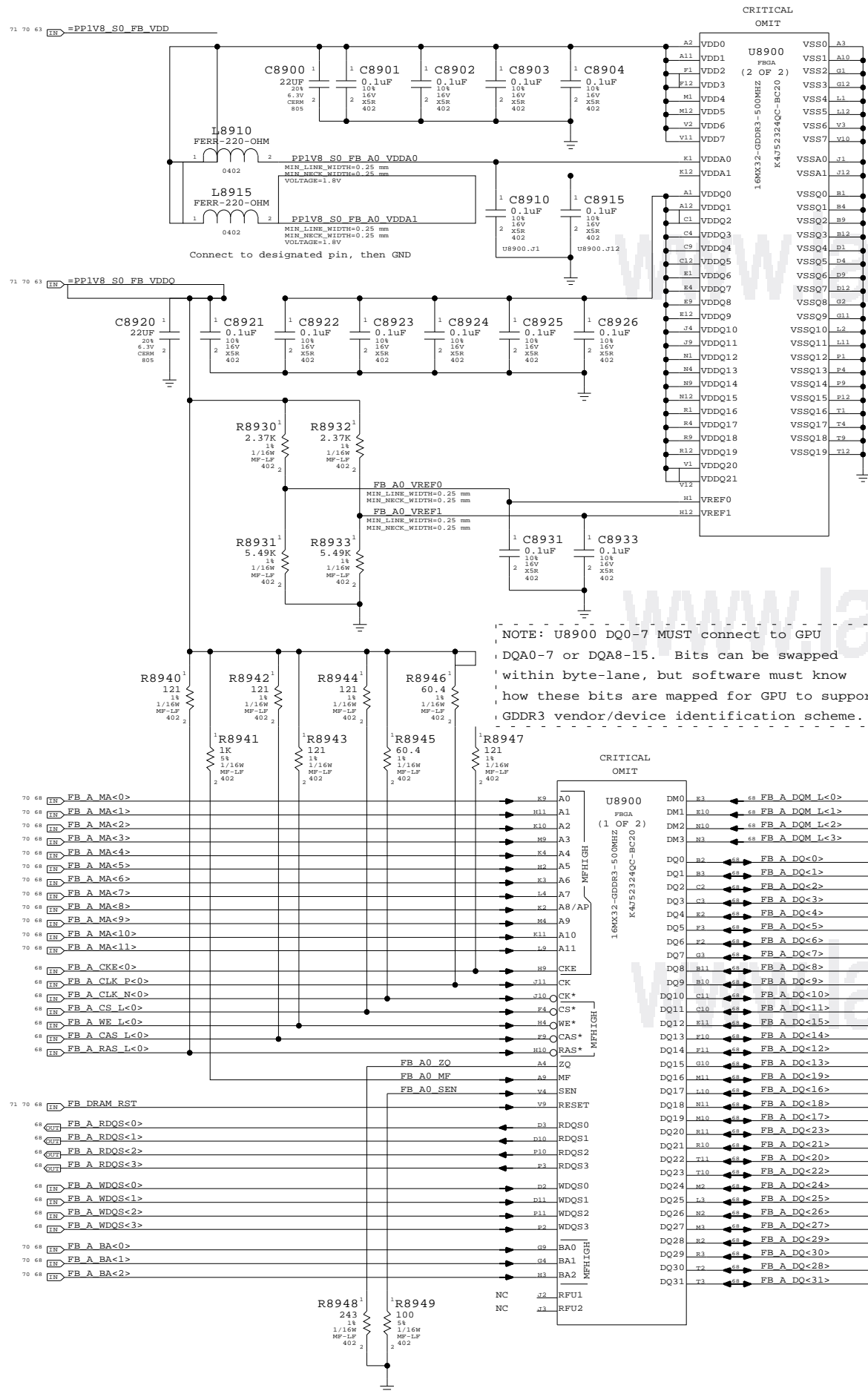




Power aliases required by this page:  
 - =PPIV8\_S0\_FB\_VDD  
 - =PPIV8\_S0\_FB\_VDDQ

Signal aliases required by this page:  
 (NONE)

BOM options provided by this page:  
 (NONE)



# GDDR3 Frame Buffer A

SYNC\_MASTER=(MASTER) SYNC\_DATE=(MASTER)

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SIZE	DRAWING NUMBER	REV.
D	051-7181	B
SCALE	SHT	OF
NONE	89	105



Power aliases required by this page:  
 - =PPIV8\_S0\_FB\_VDD  
 - =PPIV8\_S0\_FB\_VDDQ

Signal aliases required by this page:  
 (NONE)

BOM options provided by this page:  
 (NONE)

GDDR3 Frame Buffer B

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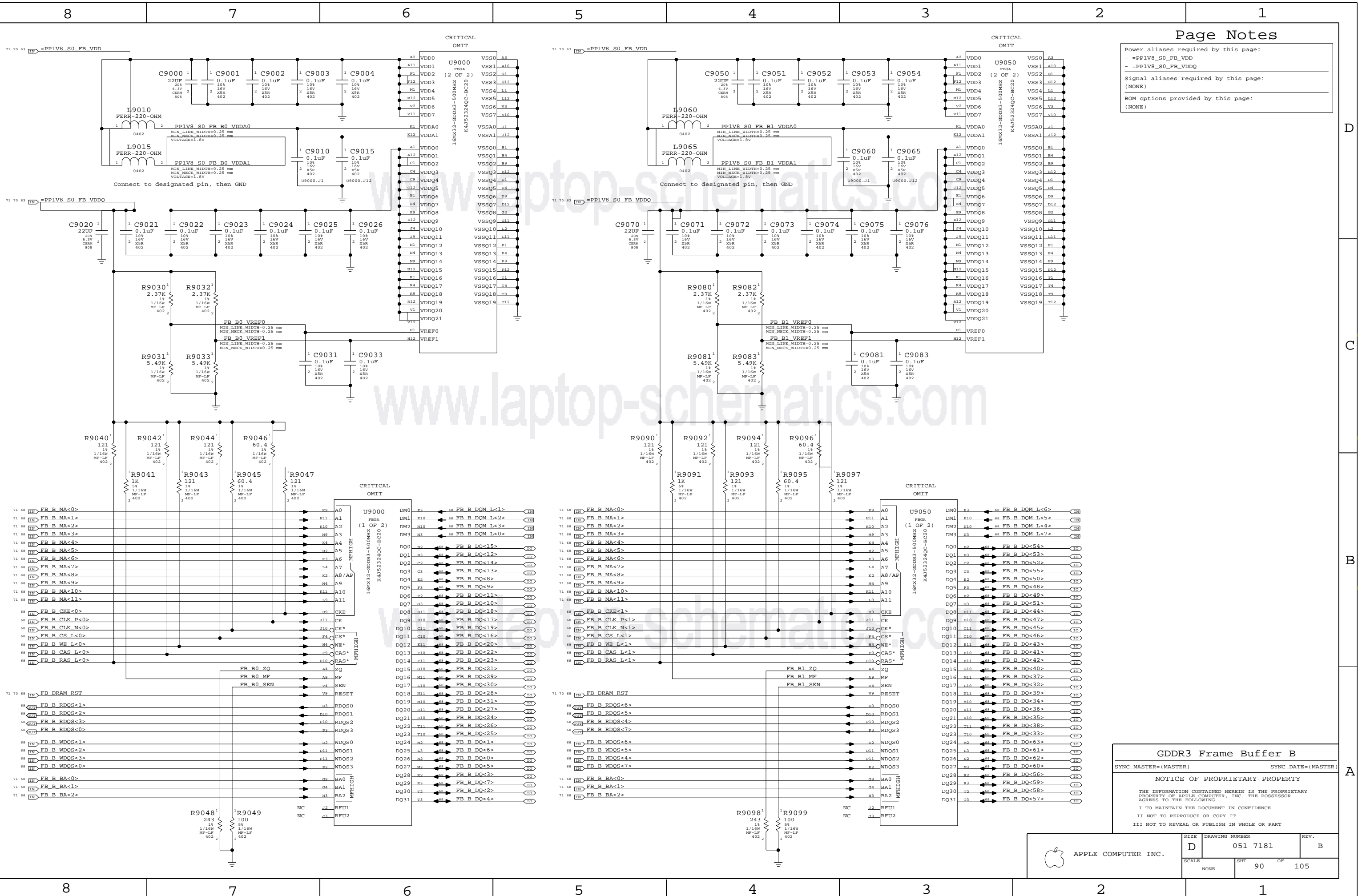
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Power aliases required by this page:

- PP3V3\_GPU\_GPIOS
- PP2V5\_PVDD
- PP1V8\_GPU\_LVDS\_PLL

---

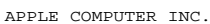
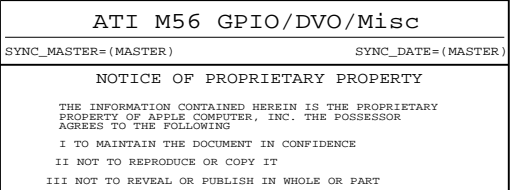
Signal aliases required by this page:

- I2C\_GPU\_TMSD\_SDA - I2C data line for external TMSD transmitters
- I2C\_GPU\_TMSD\_SCL - I2C clock line for external TMSD transmitters

---

BOM options provided by this page:

(NONE)



REV.

## Page Notes

Power aliases required by this page:

- =PP2V5\_S0\_GPU  
- =PP1V8R2V5\_S0\_GPU\_LVDDR

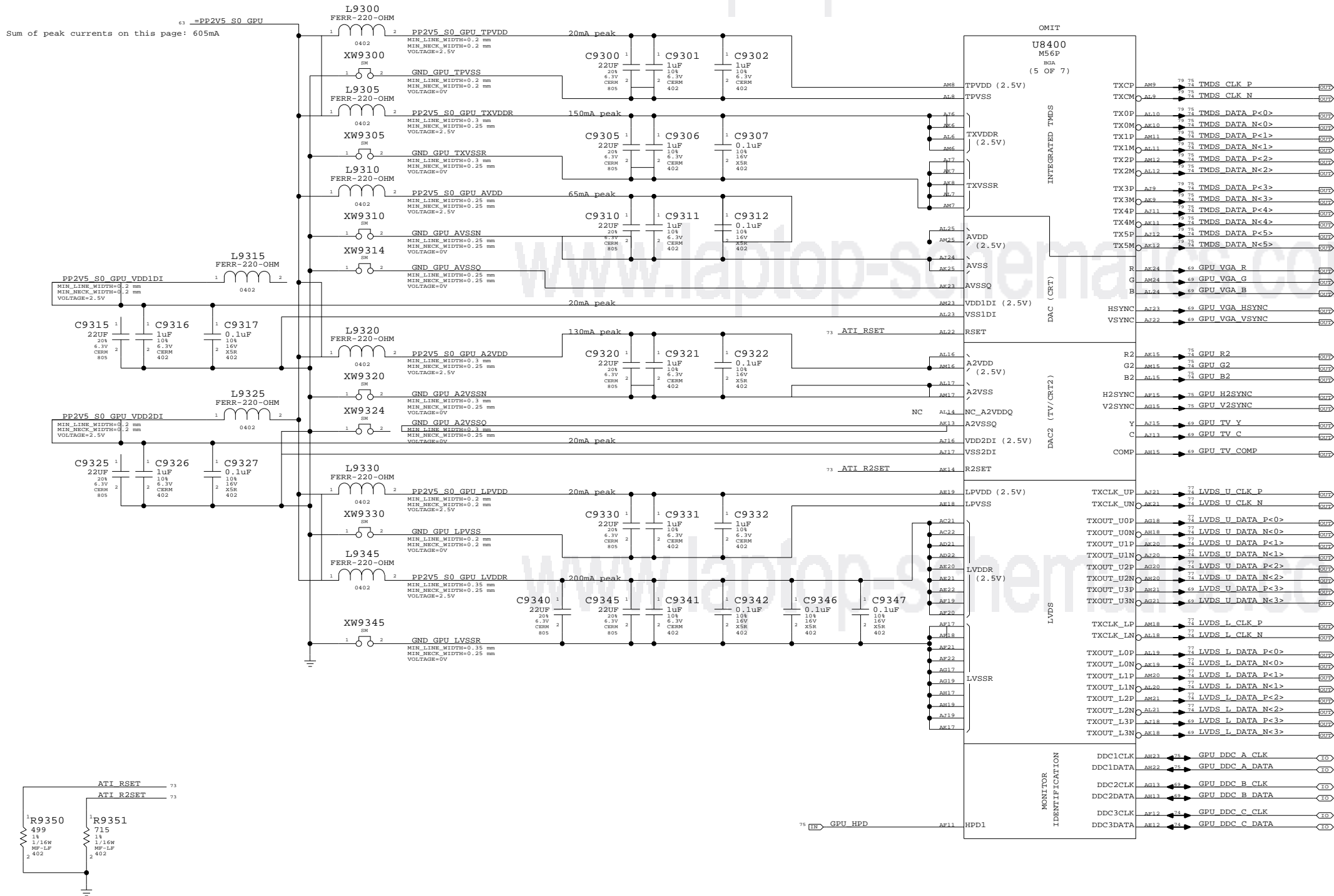
Signal aliases required by this page:

(NONE)

BOM options provided by this page:

(NONE)

Sum of peak currents on this page: 605mA



## ATI M56 Video Interfaces

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SIZE

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SCALE

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DRAWING NUMBER

051-7181

SHT

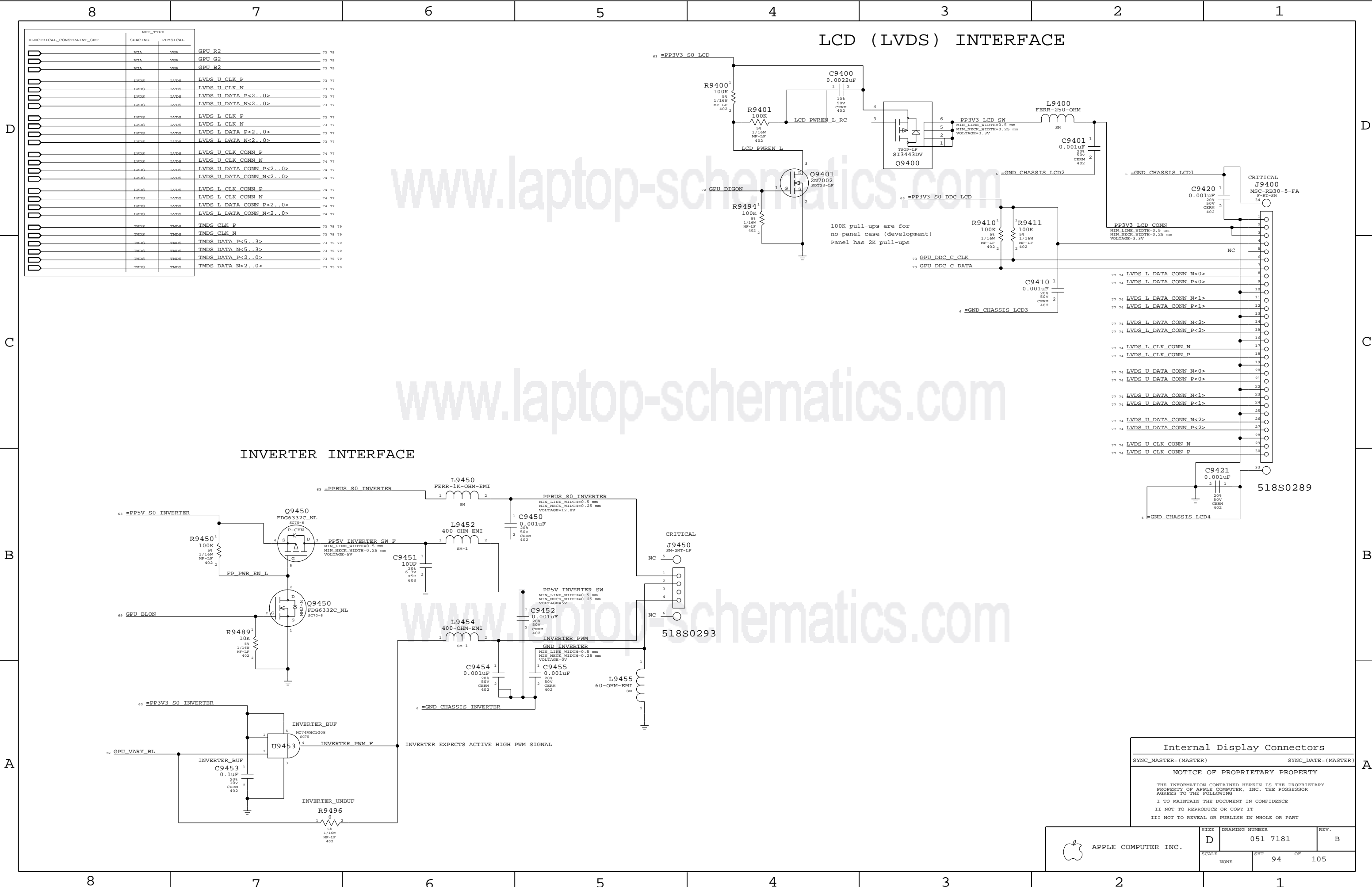
93

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105

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B



Internal Display Connectors

SYNC\_MASTER=(MASTER) SYNC\_DATE=(MASTER)

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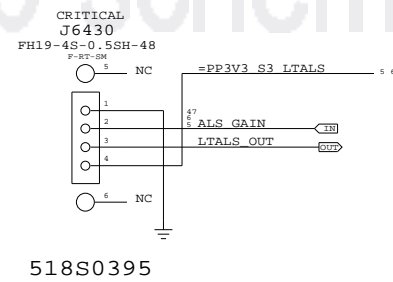
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II NOT TO REPRODUCE OR COPY IT

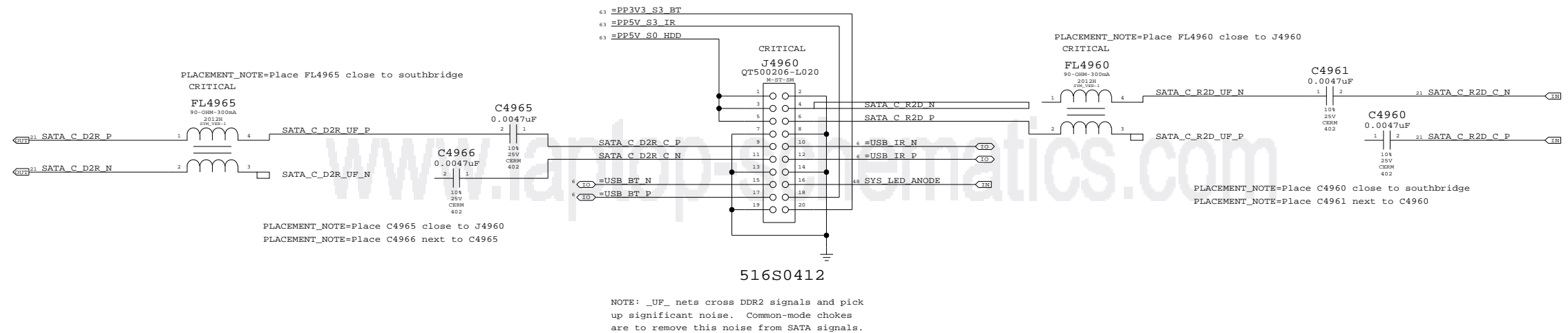
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART








## Bluetooth (M13P), IR & SATA HDD Flex Connector



M1 Specific Connectors	
SYNC_MASTER=(MASTER)	SYNC_DATE=(MASTER)
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	D	051-7181	B
	SCALE	SHT OF	
	NONE	98 105	





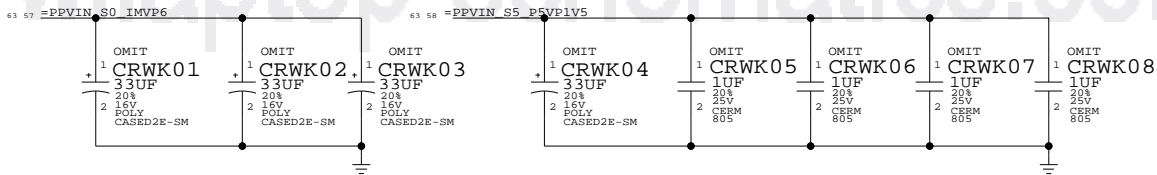


[illegible]

# ANGLED CAPS FOR C4 NOISE

## CPU AREA

RefDes	Connection to unstuffed comp. pads
CRWK01	D7500.1 to C7560.2 (poscap + end)
CRWK02	C7562.2 to C7563.1 (poscap + end)
CRWK03	C7560.2 to C7510.1 (poscap + end)
CRWK04	C7513.2 to C7640.1 (poscap + end)
CRWK05	C7680.2 to C7680.1
CRWK06	C7680.2 to C7680.1
CRWK07	C7681.1 to C7681.2
CRWK08	C7681.1 to C7681.2



(CPU VCORE, 5V/1.5V)

## GPU AREA

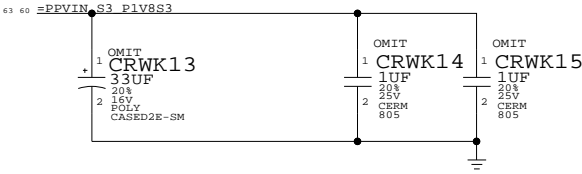
RefDes	Connection to unstuffed comp. pads
CRWK09	C7982.2 to C7980.1 (poscap + end)
CRWK10	C7982.1 to C7982.2
CRWK11	C8530.2 to C8532.1 (poscap + end)
CRWK12	C8530.1 to C8530.2



(1.05V, GPU VCORE)

## SB AREA

RefDes	Connection to unstuffed comp. pads
CRWK13	C7830.2 to C77831.1 (poscap + end)
CRWK14	C7833.2 to C7833.1
CRWK15	C7833.2 to C7833.1



(1.8V)

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
128S0092	4	CAP,TANT,POLY,33UF,16V,,070HM,D2E CASE	CRWK01,CRWK02,CRWK03,CRWK04	CRITICAL	
128S0092	3	CAP,TANT,POLY,33UF,16V,,070HM,D2E CASE	CRWK09,CRWK11,CRWK13	CRITICAL	
138S0319	4	CAP,CER,1.0UF,10%,16V,X7R,0805,SMD	CRWK05,CRWK06,CRWK07,CRWK08	CRITICAL	
138S0319	4	CAP,CER,1.0UF,10%,16V,X7R,0805,SMD	CRWK10,CRWK12,CRWK14,CRWK15	CRITICAL	

### ANGLED CAPS FOR C4 NOISE

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